mXT1067TD-AT/mXT1067TD-AB 1.0 SPI Variant

maXTouch 1066-node Touchscreen Controller

Automotive Applications

- AEC-Q100 Qualified
- Developed following Automotive SPICE® Level 3 certified processes
- CISPR 25 compliant (for both mutual and self capacitance measurements)

maXTouch® Adaptive Sensing Touchscreen Technology

- Up to 41 X (transmit) lines and 26 Y (receive) lines for use by a touchscreen and a key array (see Section 4.3 “Permitted Configurations”)
- Touchscreen size 10.51 inches (16:10 aspect ratio), assuming a sensor electrode pitch of 5.5 mm. Other sizes are possible with different electrode pitches and appropriate sensor material
- A maximum of 1066 X/Y nodes can be allocated to the touch sensor
- Multiple touch support with up to 16 concurrent touches tracked in real time

Keys

- Up to 16 nodes can be allocated as mutual capacitance sensor keys (subject to other configurations)
- Adjacent Key Suppression (AKS) technology is supported for false key touch prevention

Touch Sensor Technology

- Discrete/out-cell support including glass and PET film-based sensors
- On-cell/touch-on display support including TFT, IPS and OLED
- Synchronization with display refresh timing capability
- Support for standard (for example, Diamond) and proprietary sensor patterns (review of designs by Microchip or a Microchip-qualified touch sensor module partner is recommended)

Front Panel Material

- Works with PET or glass, including curved profiles (configuration and stack-up to be approved by Microchip or a Microchip-qualified touch sensor module partner)
- 10 mm glass (or 5 mm PMMA) with bare finger (dependent on screen size, touch size, configuration and stack-up)
- 6 mm glass (or 3 mm PMMA) with multi-finger 5 mm glove (2.7 mm PMMA equivalent) (dependent on screen size, touch size, configuration and stack-up)

Touch Performance

- Moisture/Water Compensation
  - No false touch with condensation or water drop up to 22 mm diameter
  - One-finger tracking with condensation or water drop up to 22 mm diameter
- Mutual capacitance and self capacitance measurements supported for robust touch detection
- P2P mutual capacitance measurements supported for extra sensitive multi-touch sensing
- Noise suppression technology to combat ambient and power-line noise
  - Up to 240 V_{PP} between 1 Hz and 1 kHz sinusoidal waveform
  - Up to 20 V_{PP} between 1 kHz and 1 MHz sinusoidal waveform
- Burst Frequency
  - Flexible and dynamic Tx burst frequency selection to reduce EMC disturbance
  - Controlled Tx burst frequency drift over process and temperature range
  - Configurable Tx waveform shaping to reduce emissions
- Scan Speed
  - Up to 112 Hz report rate for one finger (subject to configuration)
  - Typical report rate for 10 touches ≥85 Hz (subject to configuration)
  - Initial touch latency <20 ms for first touch from idle (subject to configuration)
  - Configurable to allow for power and speed optimization

- Touch panel failure detection
  - Automatic touch sensor diagnostics during run time to support the implementation of safety critical features
  - Diagnostics reported using dedicated output pin or by standard Object Protocol messages
  - Configurable test limits

Enhanced Algorithms

- Lens bending algorithms to remove display noise
- Touch suppression algorithms to remove unintentional large touches, such as palm
- Palm Recovery Algorithm for quick restoration to normal state

Power Saving

- Programmable timeout for automatic transition from Active to Idle state
- Pipelined analog sensing detection and digital processing to optimize system power efficiency

Application Interfaces

- SPI slave (up to 8 MHz)
- Interrupt to indicate when a message is available
- Additional SPI Debug Interface to read the raw data for tuning and debugging purposes

Power Supply

- Digital (Vdd) 3.3V nominal
- Digital I/O (VddIO) 3.3V nominal
- Analog (AVdd) 3.3V nominal
- High voltage internal X line drive (XVdd) 6.6 V with internal voltage pump
  (XVdd connected to Vdd if voltage pump not used)

Package

- 128-lead TQFP 14 × 14 × 1 mm, 0.4 mm pitch

Operating Temperature

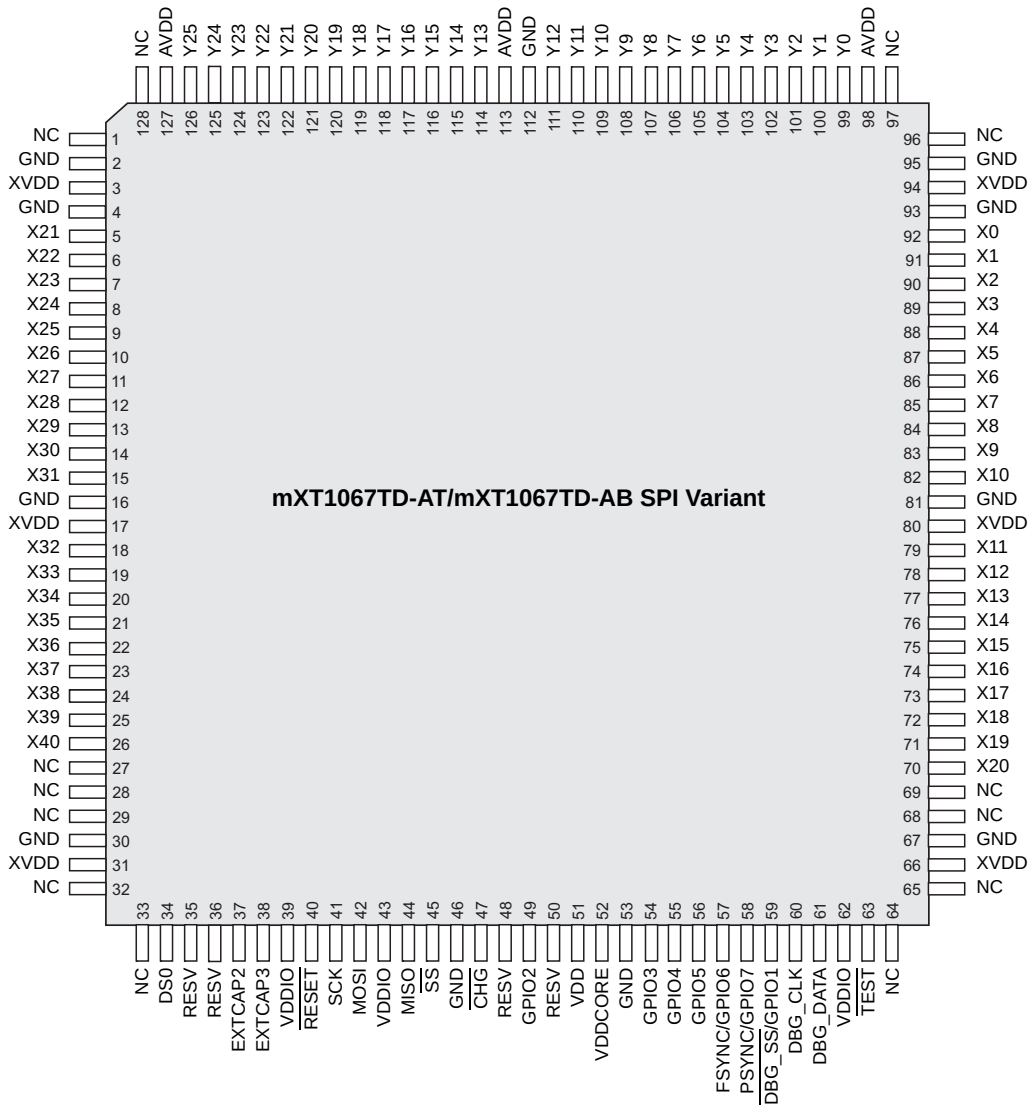
- mXT1067TD-AT SPI Variant: –40°C to +85°C (Grade 3)
- mXT1067TD-AB SPI Variant: –40°C to +105°C (Grade 2)

Design Services

- Review of device configuration, stack-up and sensor patterns
- Custom firmware versions can be considered
- Contact your Microchip representative for more information

PIN CONFIGURATION

Pin Configuration – 128-lead TQFP



Top view

TABLE 0-1: PIN LISTING – 128-LEAD TQFP

Pin	Name	Type	Supply	Description	If Unused...
1	NC	–	–	No connection	–
2	GND	P	–	Ground	–
3	XVDD	P	–	X line drive power	–
4	GND	P	–	Ground	–
5	X21	S	XVdd	X line connection	Leave open
6	X22	S	XVdd	X line connection	Leave open
7	X23	S	XVdd	X line connection	Leave open
8	X24	S	XVdd	X line connection	Leave open
9	X25	S	XVdd	X line connection	Leave open
10	X26	S	XVdd	X line connection	Leave open
11	X27	S	XVdd	X line connection	Leave open
12	X28	S	XVdd	X line connection	Leave open
13	X29	S	XVdd	X line connection	Leave open
14	X30	S	XVdd	X line connection	Leave open
15	X31	S	XVdd	X line connection	Leave open
16	GND	P	–	Ground	–
17	XVDD	P	–	X line drive power	–
18	X32	S	XVdd	X line connection	Leave open
19	X33	S	XVdd	X line connection	Leave open
20	X34	S	XVdd	X line connection	Leave open
21	X35	S	XVdd	X line connection	Leave open
22	X36	S	XVdd	X line connection	Leave open
23	X37	S	XVdd	X line connection	Leave open
24	X38	S	XVdd	X line connection	Leave open
25	X39	S	XVdd	X line connection	Leave open
26	X40	S	XVdd	X line connection	Leave open
27	NC	–	–	No connection	–
28	NC	–	–	No connection	–
29	NC	–	–	No connection	–
30	GND	P	–	Ground	–
31	XVDD	P	–	X line drive power	–
32	NC	–	–	No connection	–
33	NC	–	–	No connection	–
34	DS0	O	AVdd	Driven Shield signal; used as guard track between X/Y signals and ground	Leave open
35	RESV	–	–	Reserved for future use	Leave open
36	RESV	–	–	Reserved for future use	Leave open
37	EXTCAP2	P	–	Connect to EXTCAP3 via capacitor; see Section 2.2.4 “Internal Voltage Pump”	Leave open
38	EXTCAP3	P	–	Connect to EXTCAP2 via capacitor; see Section 2.2.4 “Internal Voltage Pump”	Leave open
39	VDDIO	P	–	Digital power	–

TABLE 0-1: PIN LISTING – 128-LEAD TQFP (CONTINUED)

Pin	Name	Type	Supply	Description	If Unused...
40	$\overline{\text{RESET}}$	I	VddIO	Reset low. Connection to host system is recommended	Pull up to VddIO
41	SCK	I	VddIO	SPI clock	–
42	MOSI	I	VddIO	SPI Mode: SPI data – Master Output Slave Input	–
43	VDDIO	P	–	Digital power	–
44	MISO	O	VddIO	SPI Mode: SPI data – Master Input Slave Output	–
45	$\overline{\text{SS}}$	O	VddIO	SPI Mode: slave select (active low)	Input: connect to GND Output: leave open
46	GND	P	–	Ground	–
47	$\overline{\text{CHG}}$	OD	VddIO	State change interrupt Note: Briefly set (~100 ms) as an input after power-up/ reset for diagnostic purposes	Pull up to VddIO
48	RESV	–	–	Reserved for future use; connect to GND	Connect to GND
49	GPIO2	I/O	VddIO	General purpose I/O; see Section 2.2.8 “GPIO Pins”	Input: connect to GND Output: leave open
50	RESV	–	VddIO	Reserved for future use; connect to GND	Connect to GND
51	VDD	P	–	Digital power	–
52	VDDCORE	P	–	Digital core power	–
53	GND	P	–	Ground	–
54	GPIO3	I/O	VddIO	General purpose I/O; see Section 2.2.8 “GPIO Pins”	Input: connect to GND Output: leave open
55	GPIO4	I/O	VddIO	General purpose I/O; see Section 2.2.8 “GPIO Pins”	Input: connect to GND Output: leave open
56	GPIO5	I/O	VddIO	General purpose I/O; see Section 2.2.8 “GPIO Pins”	Input: connect to GND Output: leave open
57	FSYNC	I	VddIO	External frame synchronization (usually VSYNC)	Input: connect to GND Output: leave open
	GPIO6	I/O		General purpose I/O; see Section 2.2.8 “GPIO Pins”	
58	PSYNC	I	VddIO	External pulse synchronization (usually HSYNC)	Input: connect to GND Output: leave open
	GPIO7	I/O		General purpose I/O; see Section 2.2.8 “GPIO Pins”	
59	$\overline{\text{DBG\_SS}}$	O	VddIO	Debug SS line; pull up to VddIO; see Section 2.2.9 “SPI Debug Interface”	Connect to test point leave open
	GPIO1	I/O		General purpose I/O; see Section 2.2.8 “GPIO Pins”	
60	DBG_CLK	O	VddIO	Debug clock; see Section 2.2.9 “SPI Debug Interface”	Connect to test point leave open
61	DBG_DATA	O	VddIO	Debug data; see Section 2.2.9 “SPI Debug Interface”	Connect to test point leave open
62	VDDIO	P	–	Digital power	–
63	$\overline{\text{TEST}}$	–	VddIO	Reserved; must be pulled up to VddIO	–
64	NC	–	–	No connection	–
65	NC	–	–	No connection	–
66	XVDD	P	–	X line drive power	–
67	GND	P	–	Ground	–
68	NC	–	–	No connection	–
69	NC	–	–	No connection	–
70	X20	S	XVdd	X line connection	Leave open

TABLE 0-1: PIN LISTING – 128-LEAD TQFP (CONTINUED)

Pin	Name	Type	Supply	Description	If Unused...
71	X19	S	XVdd	X line connection	Leave open
72	X18	S	XVdd	X line connection	Leave open
73	X17	S	XVdd	X line connection	Leave open
74	X16	S	XVdd	X line connection	Leave open
75	X15	S	XVdd	X line connection	Leave open
76	X14	S	XVdd	X line connection	Leave open
77	X13	S	XVdd	X line connection	Leave open
78	X12	S	XVdd	X line connection	Leave open
79	X11	S	XVdd	X line connection	Leave open
80	XVDD	P	–	X line drive power	–
81	GND	P	–	Ground	–
82	X10	S	XVdd	X line connection	Leave open
83	X9	S	XVdd	X line connection	Leave open
84	X8	S	XVdd	X line connection	Leave open
85	X7	S	XVdd	X line connection	Leave open
86	X6	S	XVdd	X line connection	Leave open
87	X5	S	XVdd	X line connection	Leave open
88	X4	S	XVdd	X line connection	Leave open
89	X3	S	XVdd	X line connection	Leave open
90	X2	S	XVdd	X line connection	Leave open
91	X1	S	XVdd	X line connection	Leave open
92	X0	S	XVdd	X line connection	Leave open
93	GND	P	–	Ground	–
94	XVDD	P	–	X line drive power	–
95	GND	P	–	Ground	–
96	NC	–	–	No connection	–
97	NC	–	–	No connection	–
98	AVDD	P	–	Analog power	–
99	Y0	S	AVdd	Y line connection	Leave open
100	Y1	S	AVdd	Y line connection	Leave open
101	Y2	S	AVdd	Y line connection	Leave open
102	Y3	S	AVdd	Y line connection	Leave open
103	Y4	S	AVdd	Y line connection	Leave open
104	Y5	S	AVdd	Y line connection	Leave open
105	Y6	S	AVdd	Y line connection	Leave open
106	Y7	S	AVdd	Y line connection	Leave open
107	Y8	S	AVdd	Y line connection	Leave open
108	Y9	S	AVdd	Y line connection	Leave open
109	Y10	S	AVdd	Y line connection	Leave open
110	Y11	S	AVdd	Y line connection	Leave open
111	Y12	S	AVdd	Y line connection	Leave open
112	GND	P	–	Ground	–

TABLE 0-1: PIN LISTING – 128-LEAD TQFP (CONTINUED)

Pin	Name	Type	Supply	Description	If Unused...
113	AVDD	P	–	Analog power	–
114	Y13	S	AVdd	Y line connection	Leave open
115	Y14	S	AVdd	Y line connection	Leave open
116	Y15	S	AVdd	Y line connection	Leave open
117	Y16	S	AVdd	Y line connection	Leave open
118	Y17	S	AVdd	Y line connection	Leave open
119	Y18	S	AVdd	Y line connection	Leave open
120	Y19	S	AVdd	Y line connection	Leave open
121	Y20	S	AVdd	Y line connection	Leave open
122	Y21	S	AVdd	Y line connection	Leave open
123	Y22	S	AVdd	Y line connection	Leave open
124	Y23	S	AVdd	Y line connection	Leave open
125	Y24	S	AVdd	Y line connection	Leave open
126	Y25	S	AVdd	Y line connection	Leave open
127	AVDD	P	–	Analog power	–
128	NC	–	–	No connection	–

Key:

I	Input only	O	Output only	I/O	Input or output
OD	Open drain output	P	Ground or power	S	Sense pin

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1.0 OVERVIEW OF MXT1067TD-AT/MXT1067TD-AB SPI VARIANT

The Microchip maXTouch family of touch controllers brings industry-leading capacitive touch performance to customer automotive applications. The mXT1067TD-AT/mXT1067TD-AB SPI Variant (known as mXT1067TD-Ax SPI Variant) features the latest generation of Microchip adaptive sensing technology that utilizes a hybrid mutual and self capacitive sensing system in order to deliver unparalleled touch features and a robust user experience.

- **Patented capacitive sensing method** – The mXT1067TD-Ax SPI Variant uses a unique charge-transfer acquisition engine to implement Microchip's patented capacitive sensing method. Coupled with a state-of-the-art CPU, the entire touchscreen sensing solution can measure, classify and track a number of individual finger touches with a high degree of accuracy in the shortest response time.
- **Capacitive Touch Engine (CTE)** – The mXT1067TD-Ax SPI Variant features an acquisition engine that uses an optimal measurement approach to ensure almost complete immunity from parasitic capacitance on the receiver input lines. The engine includes sufficient dynamic range to cope with anticipated touchscreen self and mutual capacitances, which allows great flexibility for use with the Microchip proprietary sensor pattern designs. One- and two-layer ITO sensors are possible using glass or PET substrates.
- **Touch detection** – The mXT1067TD-Ax SPI Variant allows for both mutual and self capacitance measurements, with the self capacitance measurements being used to augment the mutual capacitance measurements to produce reliable touch information.

  When self capacitance measurements are enabled, touch classification is achieved using both mutual and self capacitance touch data. This has the advantage that both types of measurement systems can work together to detect touches under a wide variety of circumstances.

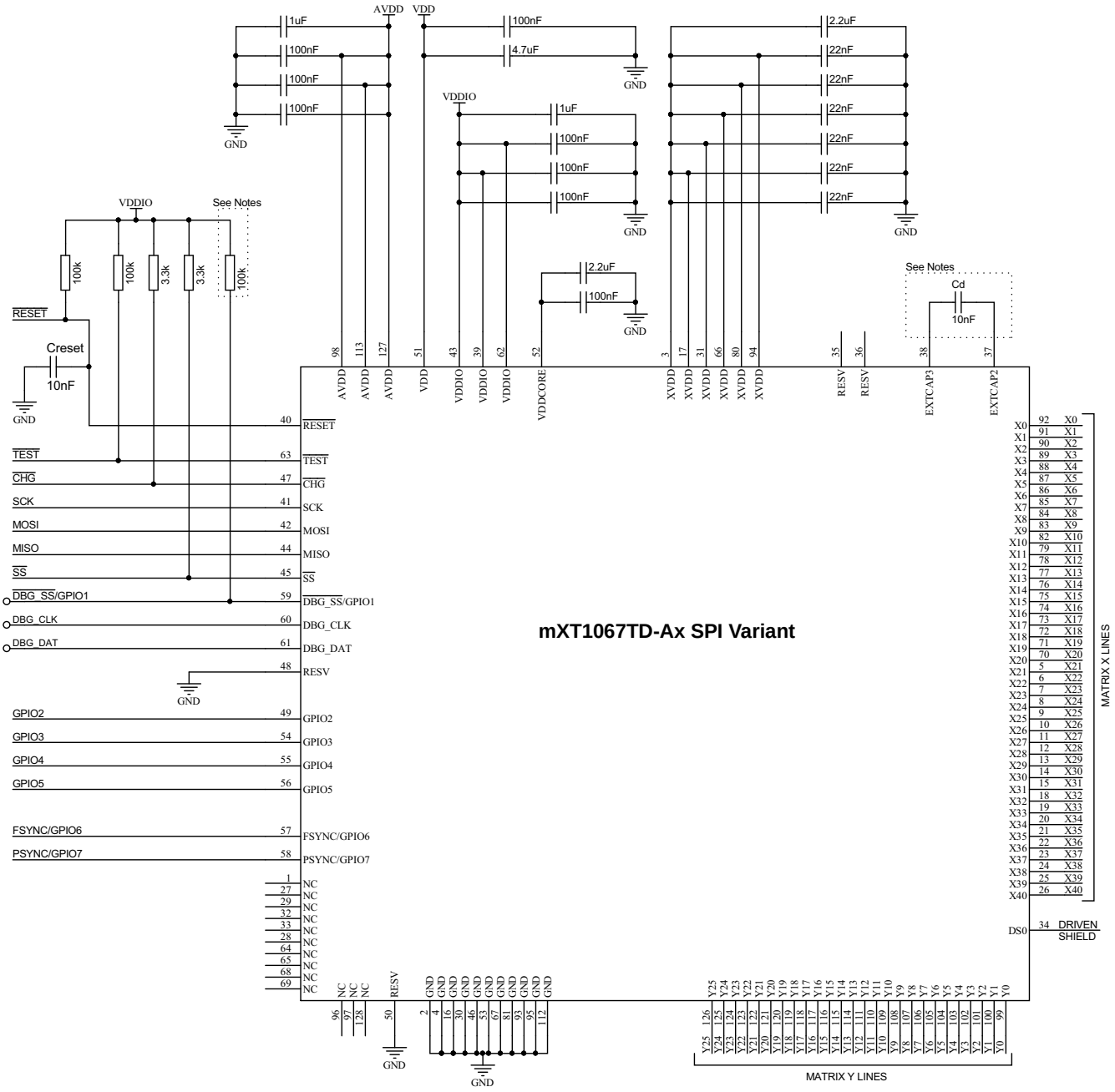
  The system may be configured for different types of default measurements in both idle and active modes. For example, the device may be configured for Mutual Capacitance Touch as the default in active mode and Self Capacitance Touch as the default in idle mode. Note that other types of scans (such as P2P mutual capacitance scans and other types of self capacitance scans) may also be made depending on configuration.

  Mutual capacitance touch data is used wherever possible to classify touches as this has greater granularity than self capacitance measurements and provides positional information on touches. For this reason, multiple touches can only be determined by mutual capacitance touch data. In Self Capacitance Touch Default mode, if the self capacitance touch processing detects multiple touches, touchscreen processing is skipped until mutual capacitance touch data is available.

  Self capacitance and P2P mutual capacitance measurements allow for the detection of touches in extreme cases, such as thick glove touches, when mutual capacitance touch detection alone may miss touches.
- **Display Noise Cancellation** – A combination of analog circuitry, hardware noise processing, and firmware that combats display noise without requiring additional listening channels or synchronization to display timing. This enables the use of shieldless touch sensor stacks, including touch-on-lens.
- **Noise filtering** – Hardware noise processing in the capacitive touch engine provides enhanced autonomous filtering and allows a broad range of noise profiles to be handled. The result is good performance in the presence of LCD noise.
- **Processing power** – The main CPU has two powerful microsequencer coprocessors under its control consuming low power. This system allows the signal acquisition, preprocessing, postprocessing and housekeeping to be partitioned in an efficient and flexible way.
- **Interpreting user intention** – The Microchip hybrid mutual and self capacitance method provides unambiguous multitouch performance. Algorithms in the mXT1067TD-Ax SPI Variant provide optimized touchscreen position filtering for the smooth tracking of touches, responding to a user's intended touches while preventing false touches triggered by ambient noise, conductive material on the sensor surface, such as moisture, or unintentional touches from the user's resting palm or fingers.

2.0 SCHEMATIC

2.1 128-lead TQFP – SPI Variant



See Section 2.2 “Schematic Notes”.

2.2 Schematic Notes

2.2.1 POWER SUPPLY

The sense and I/O pins are supplied by the power rails on the device as listed in Table 2-1. This information is also indicated in "Pin configuration".

TABLE 2-1: POWER SUPPLY FOR SENSE AND I/O PINS

Power Supply	Pins
XVdd	X sense lines
AVdd	Y sense lines, DS0
VddIO	$\overline{\text{RESET}}$, GPIO*n*, FSYNC, PSYNC, MOSI, SCK, MISO, $\overline{\text{CHG}}$, DBG_CLK, DBG_DATA, $\overline{\text{DBG\_SS}}$

2.2.2 DECOUPLING CAPACITORS

All decoupling capacitors must be X7R or X5R and placed less than 5 mm away from the pins for which they act as bypass capacitors. Pins of the same type can share a capacitor provided no pin is more than 10 mm from the capacitor.

The schematics on the previous pages show the capacitors required. The parallel combination of capacitors is recommended to give high and low frequency filtering, which is beneficial if the voltage regulators are likely to be some distance from the device (for example, If an active tail design is used). Note that this requires that the voltage regulator supplies for AVdd, Vdd and VddIO are clean and noise free. It also assumes that the track length between the capacitors and on-board power supplies is less than 50 mm.

The number of base capacitors can be reduced if the pinout configuration means that sharing a bypass capacitor is possible (subject to the distance between the pins satisfying the conditions above and there being no routing difficulties).

2.2.3 PULL-UP RESISTORS

The pull-up resistors shown in the schematic are suggested typical values and may be modified to meet the requirements of an individual customer design.

2.2.4 INTERNAL VOLTAGE PUMP

XVdd power can be supplied using an internal voltage pump.

The voltage pump requires one external capacitor:

- EXTCAP2 must be connected to EXTCAP3 via a capacitor (Cd). The capacitor must be placed as close as possible to the EXTCAP*n* pins.
- The capacitor on XVDD should be rated at least 10 V if the voltage doubler is used.

Capacitor Cd should provide a capacitance of 10 nF.

If XVdd voltage doubler is not required:

- Capacitor Cd should be omitted and EXTCAP2 and EXTCAP3 left unconnected.
- XVDD must be connected to VDD.

2.2.5 VDDCORE

VddCore is internally generated from the Vdd power supply. To guarantee stability of the internal voltage regulator, one or more external decoupling capacitors are required.

2.2.6 DRIVEN SHIELD LINE

The driven shield line (DS0) can be used to shield the X/Y sense lines. Specifically, it acts as a driven shield in self capacitance operation. See Section 8.4 "Driven Shield Line" for more details.

NOTE	DS0 is internally multiplexed to X31. X31 must be configured for use if DS0 is to be used (either as a driven shield for self capacitance measurements or as a Ground guard track in a mutual capacitance only design), otherwise DS0 cannot be used in the user's design.

2.2.7 MULTIPLE FUNCTION PINS

Some pins may have multiple functions. In this case, only one function can be chosen and the circuit should be designed accordingly.

2.2.8 GPIO PINS

The mXT1067TD-Ax SPI Variant has 7 GPIO pins. The pins can be set to be either an input or an output, as required, using the GPIO Configuration T19 object.

If a GPIO pin is unused, it can be left unconnected externally as long as it is given a defined state by the GPIO Configuration T19 object.

By default the GPIO pins are set to be inputs so if a pin is not used, and is left configured as an input, it should be connected to GND through a resistor or else the internal resistor should be pulled up using the GPIO Configuration T19 object. Note that this does not apply if the GPIO pin is shared with a debug line; see Section 2.2.9 “SPI Debug Interface” for advice on how to treat an unused GPIO pin in this case.

Alternatively, the GPIO pin can be set as an output low using the GPIO Configuration T19 object and left open. This second option avoids any problems should the pin accidentally be configured as output high at a later date.

If the GPIO Configuration T19 object is not enabled for use, the GPIO pins cannot be used for GPIO purposes, although any alternative function can still be used.

Some GPIO pins have alternative functions. If an alternative function is used then this takes precedence over the GPIO function and the pin cannot be used as a GPIO pin. In particular:

- GPIO6 cannot be used if the FSYNC function is in use
- GPIO7 cannot be used if the PSYNC function is in use
- The SPI Debug Interface functionality is shared with some of the GPIO pins. See Section 2.2.9 “SPI Debug Interface” for more details on the SPI Debug Interface and how to handle these pins if they are totally unused.

2.2.9 SPI DEBUG INTERFACE

The DBG_CLK, DBG_DATA and $\overline{\text{DBG\_SS}}$ lines form the SPI Debug Interface. These pins should be routed to test points on all designs, such that they can be connected to external hardware during system development and for debug purposes. See also Section 10.1 “SPI Debug Interface”.

The debug lines may share pins with other functionality. If the circuit is designed to use the SPI Debug Interface, then any alternative functionality cannot be used. Specifically:

- The $\overline{\text{DBG\_SS}}$ line shares functionality with GPIO1, so GPIO1 cannot be used.
- The pull-up resistor for $\overline{\text{DBG\_SS}}$ in the schematics is optional and should be present only if the line is used as $\overline{\text{DBG\_SS}}$.

The DBG_CLK, DBG_DATA and $\overline{\text{DBG\_SS}}$ lines should not be connected to power or GND. For this reason, where these pins are shared with GPIO pins and they are totally unused (that is, they are not being used as debug or GPIO pins), they should be set as outputs using the GPIO Configuration T19 object.

3.0 TOUCHSCREEN BASICS

3.1 Sensor Construction

A touchscreen is usually constructed from a number of transparent electrodes. These are typically on a glass or plastic substrate. They can also be made using non-transparent electrodes, such as copper or carbon. Electrodes are constructed from Indium Tin Oxide (ITO) or metal mesh. Thicker electrodes yield lower levels of resistance (perhaps tens to hundreds of Ω/square) at the expense of reduced optical clarity. Lower levels of resistance are generally more compatible with capacitive sensing. Thinner electrodes lead to higher levels of resistance (perhaps hundreds to thousands of Ω/square) with some of the best optical characteristics.

Interconnecting tracks can cause problems. The excessive RC time constants formed between the resistance of the track and the capacitance of the electrode to ground can inhibit the capacitive sensing function. In such cases, the tracks should be replaced by screen printed conductive inks (non-transparent) outside the touchscreen viewing area.

3.2 Electrode Configuration

The specific electrode designs used in Microchip touchscreens are the subject of various patents and patent applications. Further information is available on request.

The device supports various configurations of electrodes as summarized in Section 4.0 “Sensor Layout”.

3.3 Scanning Sequence

All nodes are scanned in sequence by the device. There is a full parallelism in the scanning sequence to improve overall response time. The nodes are scanned by measuring capacitive changes at the intersections formed between the first X line and all the Y lines. Then the intersections between the next X line and all the Y lines are scanned, and so on, until all X and Y combinations have been measured.

The device can be configured in various ways. It is possible to disable some nodes so that they are not scanned at all. This can be used to improve overall scanning time.

3.4 Touchscreen Sensitivity

3.4.1 ADJUSTMENT

Sensitivity of touchscreens can vary across the extents of the electrode pattern due to natural differences in the parasitic capacitance of the interconnections, control chip, and so on. An important factor in the uniformity of sensitivity is the electrode design itself. It is a natural consequence of a touchscreen pattern that the edges form a discontinuity and hence tend to have a different sensitivity. The electrodes at the far edges do not have a neighboring electrode on one side and this affects the electric field distribution in that region.

A sensitivity adjustment is available for the whole touchscreen. This adjustment is a basic algorithmic threshold that defines when a node is considered to have enough signal change to qualify as being in detect.

3.4.2 MECHANICAL STACKUP

The mechanical stackup refers to the arrangement of material layers that exist above and below a touchscreen. The arrangement of the touchscreen in relation to other parts of the mechanical stackup has an effect on the overall sensitivity of the screen. QMatrix technology has an excellent ability to operate in the presence of ground planes close to the sensor. QMatrix sensitivity is attributed more to the interaction of the electric fields between the transmitting (X) and receiving (Y) electrodes than to the surface area of these electrodes. For this reason, stray capacitance on the X or Y electrodes does not strongly reduce sensitivity.

Front panel dielectric material has a direct bearing on sensitivity. Plastic front panels are usually suitable up to about 5 mm, and glass up to about 10 mm (dependent upon the screen size and layout). The thicker the front panel, the lower the signal-to-noise ratio of the measured capacitive changes and hence the lower the resolution of the touchscreen. In general, glass front panels are near optimal because they conduct electric fields almost twice as easily as plastic panels.

NOTE	Care should be taken using ultra-thin glass panels as retransmission effects can occur, which can significantly degrade performance.

4.0 SENSOR LAYOUT

NOTE	The specific electrode designs used in Microchip touchscreens may be the subject of various patents and patent applications. Further information is available on request.

4.1 Electrodes

The device supports various configurations of touch electrodes as summarized below:

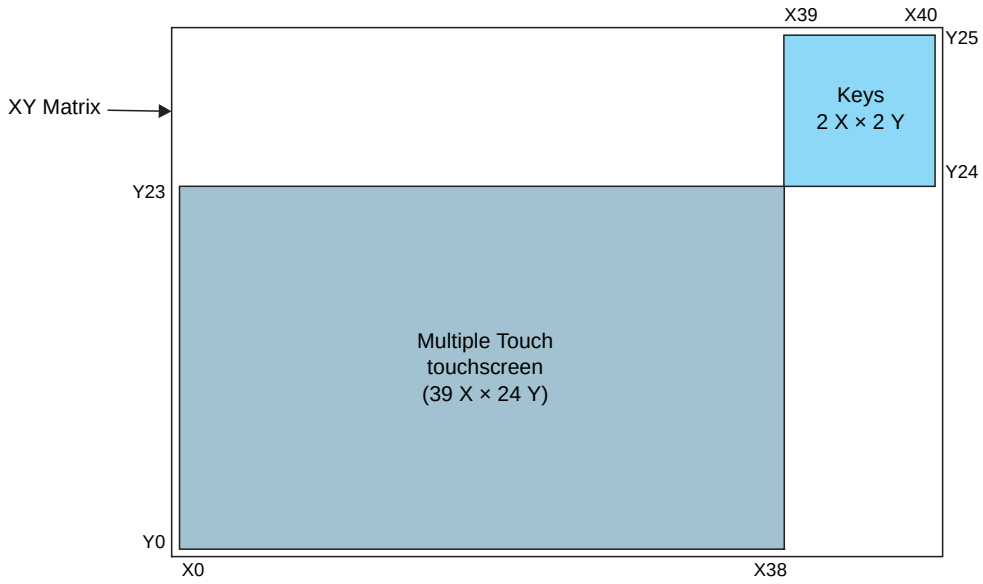
- Touchscreen: 1 touchscreen panel occupies a rectangular matrix of up to 41 X × 26 Y lines maximum (subject to other configurations).
- Keys: Up to 16 keys in an X/Y grid (Key Array), with each node (X/Y intersection) forming a key within the array.

The physical sensor matrix is configured using one or more touch objects. It is not mandatory to have all the allowable touch objects on the device enabled, so objects that are not required can be left disabled (default).

4.2 Sensor Matrix Layout

An example layout is shown in Figure 4-1.

FIGURE 4-1: EXAMPLE LAYOUT



When designing the physical layout of the touch panel, the following rules must be obeyed:

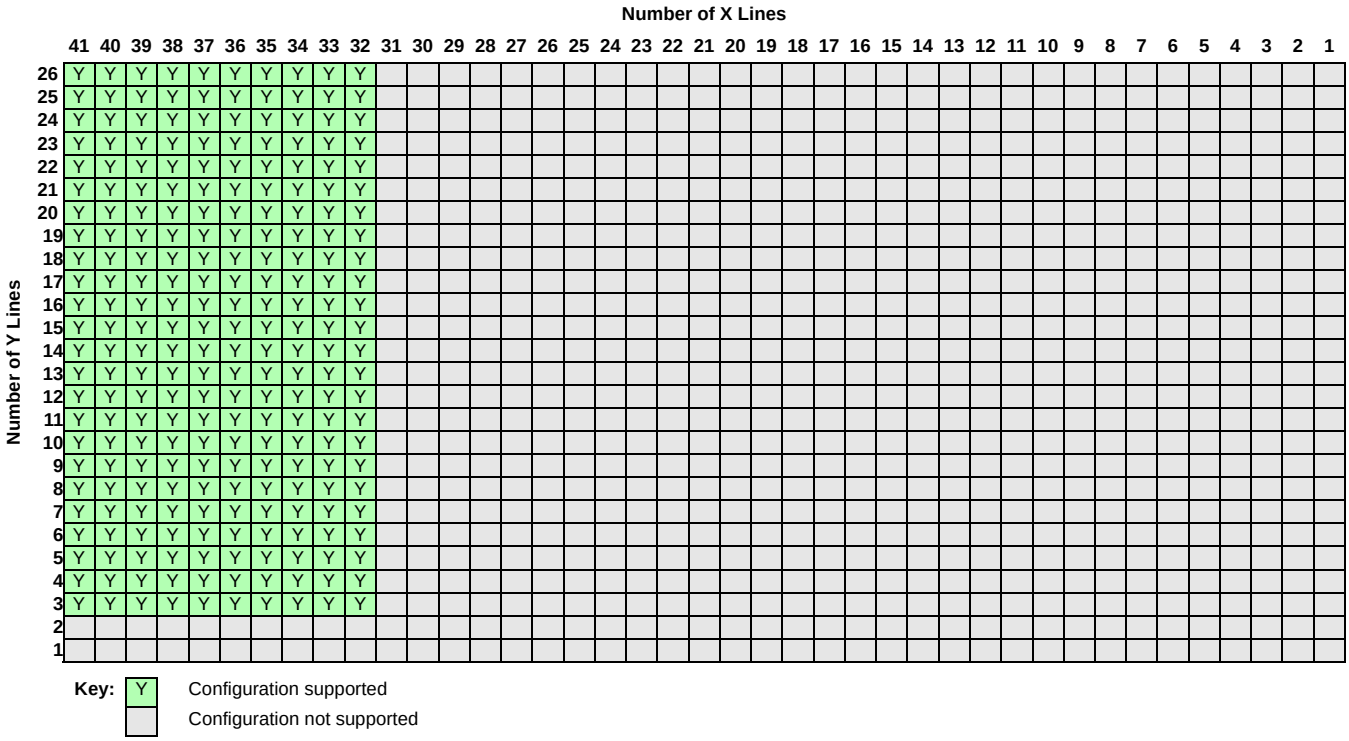
- **General layout rules:**
  - Each touch object should be a regular rectangular shape in terms of the lines it uses.
  - X31 is connected internally to the driven shield line (DS0). The driven shield does not function if X31 is not used for self capacitance measurements. X31 must therefore be included within the sensor matrix if the driven shield is used.
  - Although each touch object must use a contiguous block of X or Y lines, there can be gaps between the blocks of X and Y lines used for the different touch objects
- **Additional layout rules for Multiple Touch Touchscreen T100:**
  - The Multiple Touch Touchscreen T100 object ***must*** start at (X0, Y0)
  - The Multiple Touch Touchscreen T100 object cannot share an X or Y line with another touch object (for example, a Key Array T15).
  - The touchscreen must contain a minimum of 3 X lines for mutual capacitance measurements. If Dual X Drive is enabled for use in the Noise Suppression T72 object, the minimum is 4 X lines. If self capacitance measurements are enabled in the Acquisition Configuration T8 object, the minimum is 6 X lines.
  - The touchscreen must contain a minimum of 3 Y lines.

- **Additional layout rules for Key Array T15:**
  - The Key Array must occupy higher X and Y lines than those used by the Multiple Touch Touchscreen T100 object.

4.3 Permitted Configurations

The permitted X/Y configurations are shown in Table 4-1.

TABLE 4-1: PERMITTED TOUCHSCREEN CONFIGURATIONS



4.4 Screen Size

Table 4-2 lists some typical screen size and electrode pitch combinations to achieve various aspect ratios.

TABLE 4-2: TYPICAL SCREEN SIZES

Aspect Ratio	Matrix Size	Node Count	Screen Diagonal (Inches)			
			4.5 mm Pitch	5 mm Pitch	5.5 mm Pitch	6 mm Pitch
Single Touchscreen (1)						
16:10	X = 41, Y = 26	1066	8.6	9.56	10.51	11.47
16:9	X = 41, Y = 23	943	8.33	9.25	10.18	11.1
8:3	X = 41, Y = 15	615	7.73	8.59	9.45	10.31
4:3	X = 35, Y = 26	910	7.72	8.58	9.44	10.3

Note 1: The figures given in the table are for a Touchscreen and show the largest node count possible to achieve the desired aspect ratio. No provision has been made for a Key Array.

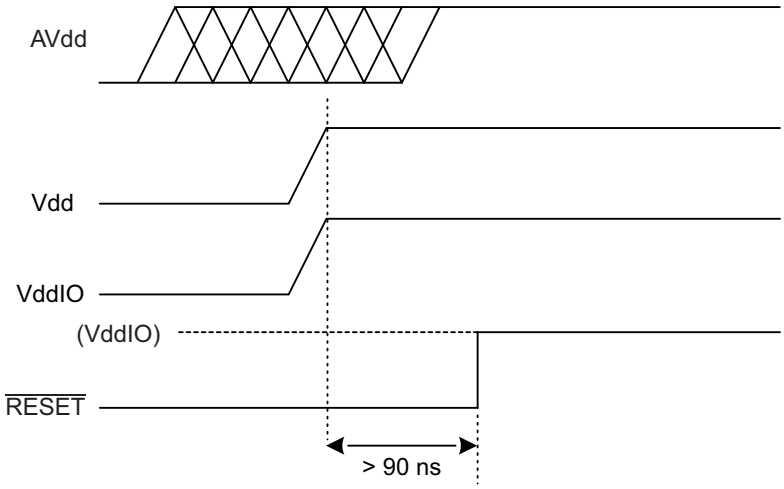
5.0 POWER-UP / RESET REQUIREMENTS

5.1 Power-on Reset

There is an internal Power-on Reset (POR) in the device.

If an external reset is to be used the device must be held in $\overline{\text{RESET}}$ (active low) while the digital (Vdd), analog (AVdd) and digital I/O (VddIO) power supplies are powering up. The supplies must have reached their nominal values before the $\overline{\text{RESET}}$ signal is deasserted (that is, goes high). This is shown in Figure 5-1. See Section 11.2 “Recommended Operating Conditions” for nominal values for the power supplies to the device.

FIGURE 5-1: POWER SEQUENCING ON THE MXT1067TD-Ax SPI VARIANT



Note: When using external $\overline{\text{RESET}}$ at power-up, VddIO must not be enabled after Vdd

It is recommended that customer designs include the capability for the host to control all the maXTouch power supplies and pull the $\overline{\text{RESET}}$ line low.

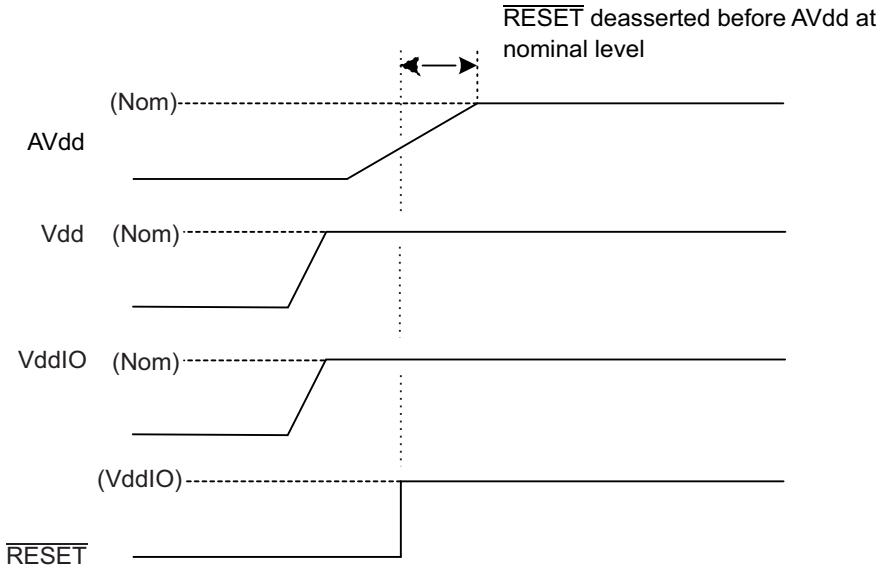
After power-up, the device typically takes 95 ms before it is ready to start communications.

NOTE	Device initialization will not complete until after all the power supplies are present. If any power supply is not present, internal initialization stalls and the device will not communicate with the host.

If the $\overline{\text{RESET}}$ line is released before the AVdd supply has reached its nominal voltage (see Figure 5-2), then some additional operations need to be carried out by the host. There are two options open to the host controller:

- Start the part in Deep Sleep mode and then send the command sequence to set the cycle time to wake the part and allow it to run normally. Note that in this case a calibration command is also needed.
- Send a RESET command.

FIGURE 5-2: POWER SEQUENCING ON THE MXT1067TD-Ax SPI VARIANT – LATE RISE ON AVDD



The RESET pin can be used to reset the device whenever necessary. The RESET pin must be asserted low for at least 90 ns to cause a reset. After the host has released the RESET pin, the device typically takes 95 ms before it is ready to start communications. It is recommended to connect the RESET pin to a host controller to allow the host to initiate a full hardware reset without requiring the mXT1067TD-Ax SPI Variant to be powered down.

WARNING	The device should be reset only by using the RESET line. If an attempt is made to reset by removing the power from the device without also sending the signal lines low, power will be drawn from the communication and I/O lines and the device will not reset correctly.

Make sure that any lines connected to the device are below or equal to Vdd during power-up. For example, if RESET is supplied from a different power domain to the VDDIO pin, make sure that it is held low when Vdd is off. If this is not done, the RESET signal could parasitically couple power via the RESET pin into the Vdd supply.

NOTE	The voltage level on the RESET pin of the device must never exceed VddIO (digital supply voltage).

A software RESET command (using the Command Processor T6 object) can be used to reset the chip. A software reset typically takes 112 ms. After the chip has finished it asserts the CHG line to signal to the host that a message is available. The reset flag is set in the Command Processor T6 object message data to indicate to the host that it has just completed a reset cycle. This bit can be used by the host to detect any unexpected brownout events. This allows the host to take any necessary corrective actions, such as reconfiguration.

NOTE	The CHG line is briefly set (~100 ms) as an input during power-up or reset. It is therefore particularly important that the line should be allowed to float high via the CHG line pull-up resistor during this period. It should never be driven by the host (see Section 11.5.4 “Reset Timings”).

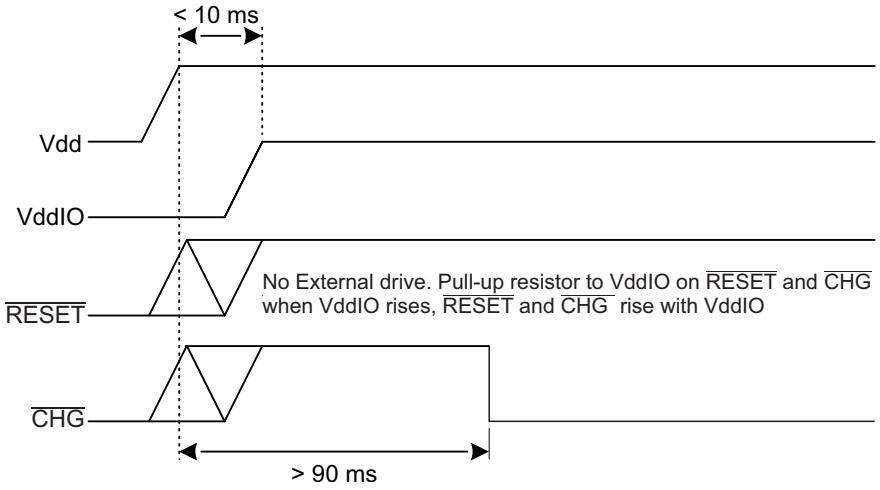
At power-on, the device performs a self-test routine (using the Self Test T25 object) to check for shorts that might cause damage to the device.

5.2 Power-up and Reset Sequence – VddIO Enabled after Vdd

The power-up sequence that can be used in applications where VddIO must be powered up after Vdd, is shown in Figure 5-3.

In this case the communication interface to the maXTouch device is not driven by the host system. The RESET and CHG pins are connected to VddIO using suitable pull-up resistors. Vdd is powered up, followed by VddIO, no more than 10 ms after Vdd. Due to the pull-up resistors, RESET and CHG will rise with VddIO. The internal POR system ensures reliable boot up of the device and the CHG line will go low approximately 95 ms after Vdd to notify the host that the device is ready to start communication.

FIGURE 5-3: POWER-UP SEQUENCE



5.3 Power-up and Initialization

The device uses a number of different power domains for optimum performance and contains circuitry to interface internal signals crossing between the different domains. There is also circuitry to ensure that the device interface logic will be initialized correctly as the device powers on. Note, however, that this does not negate specific instructions elsewhere in this section about the order that the different supplies should power up. Also, as previously mentioned, RESET should be held low until after all power rails are stable. In addition, the device will not initialize until all the voltage rails have powered up and are present.

If one domain loses power, however (for example, due to a fault or an ESD event), the device should be power-cycled to ensure that the interface logic is once again initialized. It is therefore recommended that customer designs include the capability for the host to control all the maXTouch power supplies and pull the RESET line low.

5.4 Summary

The power-up and reset requirements for the maXTouch devices are summarized in Table 5-1.

TABLE 5-1: POWER-UP AND RESET REQUIREMENTS

Condition	External RESET	VddIO Delay (After Vdd)	AVdd Power-Up	Comments
1	Low at Power-up	0 ms	Before RESET is released	If AVdd bring-up is delayed, then additional actions will be required by the host (see Section 5.1 “Power-on Reset”)
2	Not driven	<10 ms	Before VddIO	

6.0 DETAILED OPERATION

6.1 Touch Detection

The mXT1067TD-Ax SPI Variant allows for both mutual and self capacitance measurements, with the self capacitance measurements being used to augment the mutual capacitance measurements to produce reliable touch information.

When self capacitance measurements are enabled, touch classification is achieved using both mutual and self capacitance touch data. This has the advantage that both types of measurement systems can work together to detect touches under a wide variety of circumstances.

Mutual capacitance touch data is used wherever possible to classify touches as this has greater granularity than self capacitance measurements and provides positional information on touches.

Self capacitance measurements, on the other hand, allow for the detection of single touches in extreme cases, such as single thick glove touches, when touches can only be detected by self capacitance data and may be missed by mutual capacitance touch detection.

6.2 Operational Modes

The device operates in two modes: **Active** (touch detected) and **Idle** (no touches detected). Both modes operate as a series of burst cycles. Each cycle consists of a short burst (during which measurements are taken) followed by an inactive sleep period. The difference between these modes is the length of the cycles. Those in idle mode typically have longer sleep periods. The cycle length is configured using the IDLEACQINT and ACTVACQINT settings in the Power Configuration T7. In addition, an *Active to Idle Timeout* setting is provided.

6.3 Detection Integrator

The device features a touch detection integration mechanism. This acts to confirm a detection in a robust fashion. A counter is incremented each time a touch has exceeded its threshold and has remained above the threshold for the current acquisition. When this counter reaches a preset limit the sensor is finally declared to be touched. If, on any acquisition, the signal is not seen to exceed the threshold level, the counter is cleared and the process has to start from the beginning.

The detection integrator is configured using the appropriate touch objects (Multiple Touch Touchscreen T100, Key Array T15).

6.4 Sensor Acquisition

The charge time for mutual capacitance measurements is set using the Acquisition Configuration T8 object.

The device combines a number of factors together to arrive at the total acquisition time for one drive line (that is, one X line for mutual capacitance acquisitions or one axis for self capacitance acquisitions), but the maximum time to complete the acquisition must not exceed 2 ms. Furthermore, the total acquisition time for the sensor as a whole must not exceed 250 ms. If either of these conditions are not met, a SIGERR will be reported.

In addition, the following constraints apply on the mXT1067TD-Ax SPI Variant:

- The per X line mutual capacitance touch measurement and the per axis self capacitance measurement must not exceed 2 ms
- The high and low pulse periods must not exceed 38.65 µs each. This means that the maximum possible burst period is 77.34 µs (that is, a minimum frequency of 12.93 kHz). In addition, the burst period must not be less than 4 µs (that is, a maximum frequency of 250 kHz).

Unpredictable system behavior might occur if any of the above constraints are not met.

Care should be taken to configure all the objects that can affect the measurement timing so that these limits are not exceeded.

6.5 Calibration

Calibration is the process by which a sensor chip assesses the background capacitance on each node. Calibration occurs in a variety of circumstances, for example:

- When determined by the mutual capacitance recalibration process, as controlled by the Acquisition Configuration T8 object
- When determined by the self capacitance recalibration process, as controlled by the Self Capacitance Configuration T111 object
- When the Retransmission Compensation T80 object detects calibrated-in moisture has been removed
- Following a Self Capacitance Global Configuration T109 Tune command
- When the host issues a recalibrate command
- When certain configuration settings are changed

6.6 Digital Filtering and Noise Suppression

The mXT1067TD-Ax SPI Variant supports on-chip filtering of the acquisition data received from the sensor. Specifically, the Noise Suppression T72 object provides an algorithm to suppress the effects of noise (for example, from a noisy charger plugged into the user's product). This algorithm can automatically adjust some of the acquisition parameters on-the-fly to filter the Analog-to-Digital Conversions (ADCs) received from the sensor.

Additional noise suppression is provided by the Self Capacitance Noise Suppression T108 object. Similar in both design and configuration to the Noise Suppression T72 object, the Self Capacitance Noise Suppression T108 object is the noise suppression interface for self capacitance touch measurements.

Noise suppression is triggered when a noise source is detected.

- The host driver code can indicate when a noise source is present.
- The noise suppression is also triggered based on the noise levels detected using internal line measurements.The Noise Suppression T72 and Self Capacitance Noise Suppression T108 object selects the appropriate controls to suppress the noise present in the system.

6.7 EMC Reduction

The mXT1067TD-Ax SPI Variant has various mechanisms that help reduce EMC emissions and ensure that the user's product operates within the desired EMC limits:

- **Spread spectrum** – Varies the burst frequency on each measurement pulse to spread the EMC energy over the frequency domain.
- **Configurable voltage reference mode** – Allows for the selection of voltage swing of the self capacitance measurements.
- **Configurable wave shaping** – Control of the voltage modulation on self capacitance scans allows wave shaping of the edge for EMC harmonic control.

These features are configured using the CTE Configuration T46, Self Capacitance Voltage Modulation T133 and Self Capacitance Global Configuration T109 objects.

6.8 Shieldless Support and Display Noise Suppression

The mXT1067TD-Ax SPI Variant can support shieldless sensor design even with a noisy LCD.

The Optimal Integration feature is not filtering as such, but enables the user to use a shorter integration window. The integration window optimizes the amount of charge collected against the amount of noise collected, to ensure an optimal SNR. This feature also benefits the system in the presence of an external noise source. This feature is configured using the Shieldless T56 object.

Display noise suppression allows the device to overcome display noise simultaneously with external noise. This feature is based on filtering provided by the Lens Bending T65 object (see Section 6.11 "Lens Bending").

6.9 Retransmission Compensation

The device can limit the undesirable effects on the mutual capacitance touch signals caused by poor device coupling to ground, such as poor sensitivity and touch break-up. This is achieved using the Retransmission Compensation T80 object. This object can be configured to allow the touchscreen to compensate for signal degradation due to these undesirable effects. If self capacitance measurements are also scheduled, the Retransmission Compensation T80 object will use the resultant data to enhance the compensation process.

The Retransmission Compensation T80 object is also capable of compensating for water presence on the sensor if self capacitance measurements are scheduled. In this case, both mutual capacitance and self capacitance measurements are used to detect moisture and then, once moisture is detected, self capacitance measurements are used to detect single touches in the presence of moisture.

6.10 Grip Suppression

The device has grip suppression functionality to suppress false detections from a user's grip.

Self Capacitance grip suppression works by looking for characteristic shapes in the self capacitance measurement along the touchscreen boundary, and thereby distinguishing between a grip and a touch further into the sensor. Self capacitance grip suppression is configured using the Self Capacitance Grip Suppression T112 object.

6.11 Lens Bending

The device supports algorithms to eliminate disturbances from the measured signal.

When the sensor suffers from the screen deformation (lens bending) the signal values acquired by normal procedure are corrupted by the disturbance component (bend). The amount of bend depends on:

- The mechanical and electrical characteristics of the sensor
- The amount and location of the force applied by the user touch to the sensor

The Lens Bending T65 object measures the bend component and compensates for any distortion caused by the bend. As the bend component is primarily influenced by the user touch force, it can be used as a secondary source to identify the presence of a touch. The additional benefit of the Lens Bending T65 object is that it will eliminate LCD noise as well.

6.12 Glove Detection

The device has glove detection algorithms that process the measurement data received from the touchscreen classifying touches as potential gloved touches.

The Glove Detection T78 object is used to detect glove touches. In Normal Mode the Glove Detection T78 object applies vigorous glove classification to small signal touches to minimize the effect of unintentional hovering finger reporting. Once a gloved touch is found, the Glove Detection T78 object enters Glove Confidence Mode. In this mode the device expects the user to be wearing gloves so the classification process is much less stringent.

6.13 Unintentional Touch Suppression

The Touch Suppression T42 object provides a mechanism to suppress false detections from unintentional touches from a large body area, such as from a face, ear or palm. The Touch Suppression T42 object also provides Maximum Touch Suppression to suppress all touches if more than a specified number of touches has been detected. There is one instance of the Touch Suppression T42 object for each Multiple Touch Touchscreen T100 object present on the device.

6.14 Adjacent Key Suppression Technology

Adjacent Key Suppression (AKS) technology is a patented method used to detect which touch object (Multiple Touch Touchscreen T100 or Key Array T15) is touched, and to suppress touches on the other touch objects, when touch objects are located close together.

The device has two levels of AKS:

- The first level works between the touch objects (Multiple Touch Touchscreen T100 and Key Array T15). The touch objects are assigned to AKS groups. If a touch occurs within one of the touch objects in a group, then touches within other objects inside that group are suppressed. For example, if a touchscreen and a Key Array are placed in the same AKS group, then a touch in the touchscreen will suppress touches in the Key Array, and vice versa. Objects can be in more than one AKS group.

- The second level of AKS is internal AKS within an individual Key Array object. If internal AKS is enabled, then when one key is touched, touches on all the other keys within the Key Array are suppressed. Note that internal AKS is not present on other types of touch objects.

7.0 SPI COMMUNICATIONS

7.1 Communications Protocol

Communication with the device is carried out over the Serial Peripheral Interface (SPI). The host communicates with the mXT1067TD-Ax SPI Variant over the SPI using a master-slave relationship, with the mXT1067TD-Ax SPI Variant acting in slave mode.

7.2 SPI Operation

The SPI uses four logic signals:

- **Serial Clock (SCK)** – output from the host.
- **Master Output, Slave Input (MOSI)** – output from the host, input to the mXT1067TD-Ax SPI Variant. Used by the host to send data to the mXT1067TD-Ax SPI Variant.
- **Master Input, Slave Output (MISO)** – input to the host, output from the mXT1067TD-Ax SPI Variant. Used by the mXT1067TD-Ax SPI Variant to send data to the host.
- **Slave Select ($\overline{SS}$)** – active low output from the host.

In addition the following pin is used:

- **Change Line ($\overline{CHG}$)** – active low input to the host, output from the mXT1067TD-Ax SPI Variant. Used by the mXT1067TD-Ax SPI Variant to indicate that a response is ready for transmission (see Section 7.2.1 “Change Line (CHG)”) or that an OBP message is pending.

The master pulls $\overline{SS}$ low at the start of the SPI transaction and it remains low until the end of it.

At each byte, the master generates 8 clock pulses on SCK. With these 8 clock pulses, a byte of data is transmitted from the master to the slave over MOSI, most significant bit first.

Simultaneously a byte of data is transmitted from the slave to the master over MISO, also most significant bit first.

The mXT1067TD-Ax SPI Variant requires that the clock idles “high” (CPOL=1). The data on MOSI and MISO pins are set at the falling edges and sampled at the rising edges (CPHA=1). This is known as SPI Mode 3.

The mXT1067TD-Ax SPI Variant SPI interface can operate at a SCK frequency of up to 8 MHz.

NOTE	The SPI interface is used in half duplex mode, even though it is a full duplex communication bus by its nature. This simplifies the protocol, minimizes the CPU processing required and avoids possible timing critical scenarios. This means that only one of the two in/out data lines (MOSI/MISO) will be meaningful at a time. During a read operation, therefore, the host must transmit 0xFF bytes on the MOSI line while it is reading data from the slave device. Similarly, during a write operation, the host must ignore the data on the MISO line.

An SPI transaction is considered as initiated when the $\overline{SS}$ line is asserted (active low) by the host and terminated when it is deasserted. The host can abort a transfer at any time by deasserting the $\overline{SS}$ line.

7.2.1 CHANGE LINE ($\overline{CHG}$)

The $\overline{CHG}$ line is an active-low, open-drain output that is used as an interrupt to alert the host that the slave is ready to send a response or that an OBP message is pending and ready to be read from the Host.

The change line must be handled by the host as a falling edge triggered line. It must not be used a level triggered line. This avoids the situation in which the host initiates a new read/write operation (because the interrupt line is still asserted following a previous SPI transaction) but the target is not yet ready to handle it.

To prevent the host missing an interrupt, the target device can use a retriggering mechanism for the interrupt line. This guarantees that any pending message is always delivered. This mechanism must be enabled in the Communications Configuration T18 object.

7.2.2 SPI PROTOCOL OPCODES

The allowed operations and responses codes used by the SPI protocol are shown in Table 7-1.

TABLE 7-1: SPI OPCODES

Name	Value	Operation
Write Operation and Responses (see Section 7.3 “Write Operation and Responses”)		
SPI_WRITE_REQ	0x01	Write operation request
SPI_WRITE_OK	0x81	Write operation succeeded (response)
SPI_WRITE_FAIL	0x41	Write operation failed (response)
Read Operation and Responses (see Section 7.4 “Read Operation and Responses”)		
SPI_READ_REQ	0x02	Read operation request
SPI_READ_OK	0x82	Read operation succeeded (response)
SPI_READ_FAIL	0x42	Read operation failed (response)
General Responses (see Section 7.5 “General Operations”)		
SPI_INVALID_REQ	0x04	Invalid operation (response)
SPI_INVALID_CRC	0x08	Invalid CRC (response)

All the responses reported in Table 7-1 require the Interrupt line to go from inactive (deasserted) to active (asserted) before the host can read a response following an SPI_READ_REQ or SPI_WRITE_REQ operation.

7.2.3 SPI TRANSACTION HEADER

Every SPI transaction includes a 6-byte HEADER that has the format shown in Table 7-2.

TABLE 7-2: HEADER FORMAT

Byte	Field	Description
0	Opcode	Op code for the transaction
1	Address LSByte	The memory address of the slave device where the Host wants to write to or read from.
2	Address MSByte	
3	Length LSByte	The number of bytes that the host wants to write to or read from the slave device.
4	Length MSByte	
5	CRC	8-bit CRC

An 8-bit CRC is used to detect errors on the 5 bytes of the header (that is: Opcode, Address LSB, Address MSB, Length LSByte, Length MSByte) in order to prevent the writing to or reading from unwanted objects if the header gets corrupted during the SPI transfer. The 8-bit CRC algorithm is the same as that used to calculate the CRC for Message Processor T5 messages.

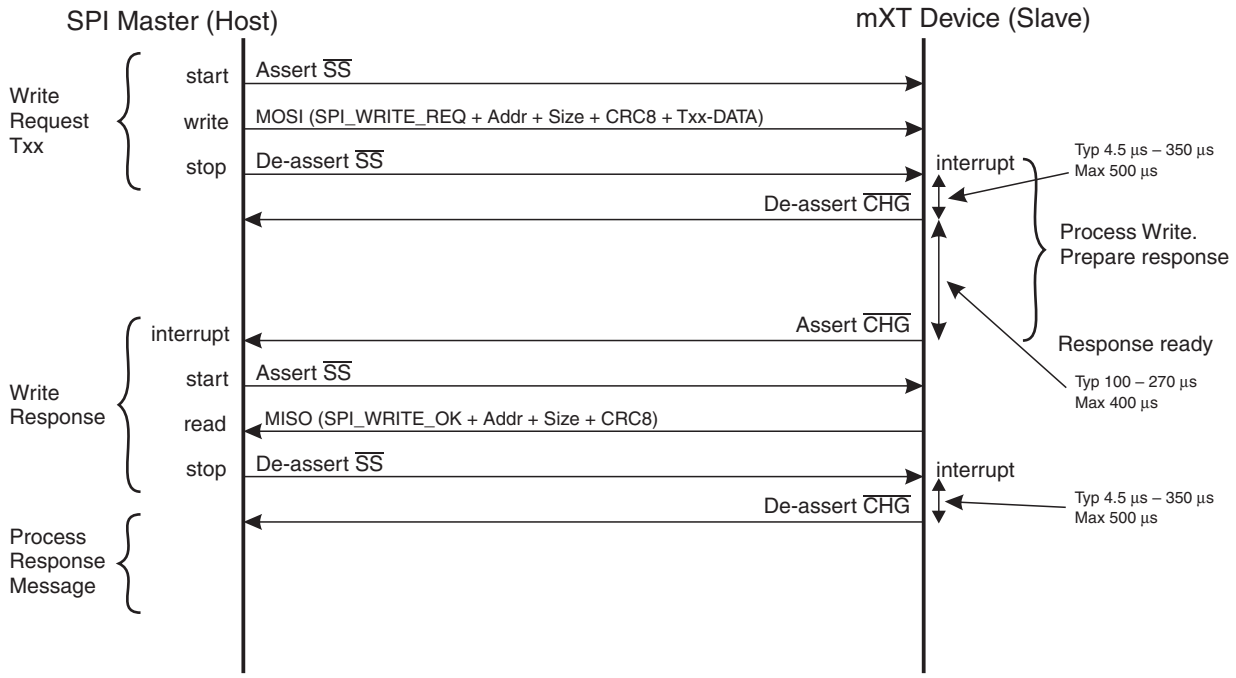
7.3 Write Operation and Responses

The write operation and its responses allows the host to write to an object configuration area.

The flow and timing are shown in Figure 7-1.

Note that no detection mechanism is provided at the SPI network layer level on the data written, but the host can check the correctness of the data that is read back by using a checksum. This allows the host to detect whether the payload of the write operation was corrupted or not during the SPI transaction (see Figure 7-5 on page 28).

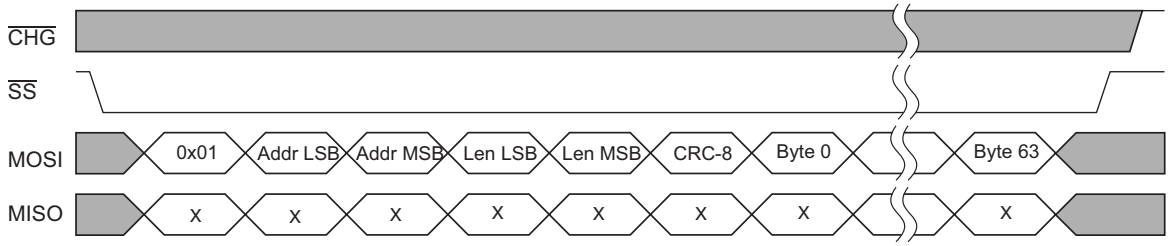
FIGURE 7-1: SPI WRITE CONFIGURATION MESSAGE FLOW AND TIMING



7.3.1 SPI_WRITE_REQ

Figure 7-2 shows the message format used for the write request operation.

FIGURE 7-2: SPI_WRITE_REQ



In Figure 7-2:

- **0x01** is the opcode
- **Addr LSB and Addr MSB** together specify the address to which the host wishes to write
- **Len LSB and Len MSB** together specify the length of the data in bytes. This is the total number of bytes that the Host wishes to write to the slave device (excluding the header bytes)
- **CRC-8** is the 8-bit CRC
- **Byte 0 .. Byte 63** contain the data that is to be written (64 bytes maximum).

If the host needs to write more than 64 bytes of data then multiple SPI_WRITE_REQ operations are required.

Following an SPI_WRITE_REQ operation, the host must wait for a response from the device before accessing the SPI bus again. If the slave system does not assert the interrupt line within 10 ms, a HW reset or a retry from the Host is necessary. When the response is ready to be sent, the target device asserts the interrupt line to notify the host that a message is ready to be read. Only at this point is the host allowed to initiate a new SPI transaction to read back the response related to the previous write operation.

This means that an object message will be blocked during the time that a response related to a previous read or write request is pending and has not yet been read back by the Host.

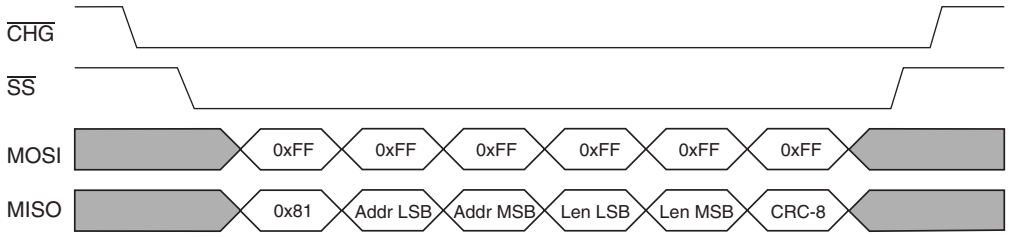
The following responses are possible following an SPI_WRITE_REQ operation:

- **SPI_WRITE_OK** – Generated if the write operation was successfully completed (the memory address and length specified by the host were within the allowed accessible memory map regions). See Section 7.3.2 “SPI_WRITE_OK”
- **SPI_WRITE_FAIL** – Generated if the write operation failed, for example if the host tries to write to an address outside the available memory map. See Section 7.3.3 “SPI_WRITE_FAIL”
- **SPI_INVALID_REQ** – See Section 7.5.1 “SPI_INVALID_REQ”
- **SPI_INVALID_CRC** – See Section 7.5.2 “SPI_INVALID_CRC”

7.3.2 SPI_WRITE_OK

Figure 7-3 shows the message format used for the write OK response.

FIGURE 7-3: SPI_WRITE_OK



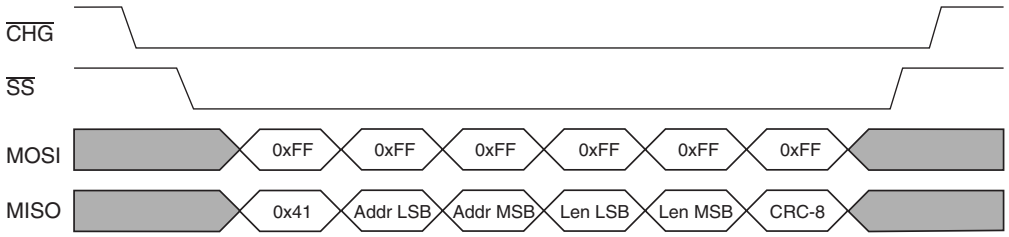
In Figure 7-3:

- **0x81** is the opcode
- **Addr LSB and Addr MSB** together specify the address to which the data was written
- **Len LSB and Len MSB** together specify the length of the data in bytes. This is the total number of bytes that was written to the slave device (excluding the header bytes)
- **CRC-8** is the 8-bit CRC

7.3.3 SPI_WRITE_FAIL

Figure 7-4 shows the message format used for the write fail response.

FIGURE 7-4: SPI_WRITE_FAIL



In Figure 7-4:

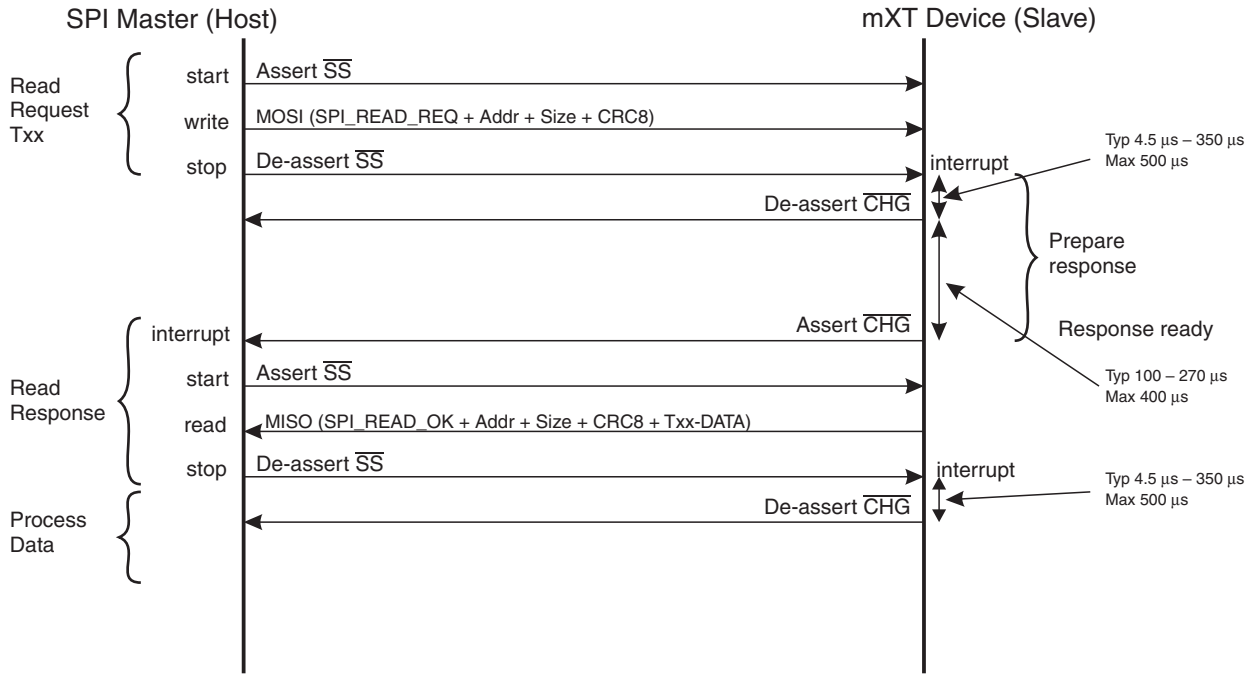
- **0x41** is the opcode
- **Addr LSB and Addr MSB** together specify the address to which the host requested the write
- **Len LSB and Len MSB** together specify the length of the data in bytes. This is the total number of bytes that the Host attempted to write to the slave device (excluding the header bytes)
- **CRC-8** is the 8-bit CRC

7.4 Read Operation and Responses

The read request operation allows the host to read from the object memory map for the device. This allows the host to read a message from the Message Processor T5 object or read from an object configuration area.

The flow and timing are shown in Figure 7-5.

FIGURE 7-5: SPI READ CONFIGURATION MESSAGE FLOW AND TIMING



Normally a limit of 64 bytes is allowed for data reads. If the host tries to read more than 64 bytes, the slave returns SPI_READ_FAIL (see Section 7.4.3 “SPI_READ_FAIL”).

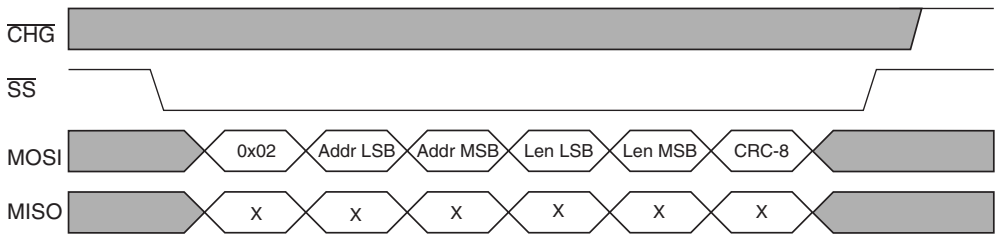
Under certain circumstances, a CRC can be used as an error detection mechanism when reading an object:

- Message Processor T5 – When reading a message from the Message Processor T5 object, an optional CRC as an error detection mechanism is provided. This is enabled in the Message Processor T5 object.
- All other objects – When reading from any other object configuration area, no error detection mechanism is provided, as this operation is typically performed only at system startup. It is possible, however, to verify a read operation by performing it twice and comparing the results.

7.4.1 SPI_READ_REQ

Figure 7-6 shows the message format used for the read request operation.

FIGURE 7-6: SPI_READ_REQ



The SPI_READ_REQ operation can be initiated by the host at any time, regardless of the state of the interrupt line. The slave device will assert the interrupt line when there are object messages pending. When the master asserts $\overline{SS}$ (whether to respond to the slave asserting the interrupt line or because the master wants to initiate a transaction), the interrupt line is deasserted until the message from the master has been received and processed.

In Figure 7-6:

- **0x02** is the opcode
- **Addr LSB and Addr MSB** together specify the address from which the host wishes to read
- **Len LSB and Len MSB** together specify the length of the data in bytes. This is the total number of bytes (excluding the header bytes) that the Host wishes to read from the slave device. The limit is 64 bytes
- **CRC-8** is the 8-bit CRC

The actual data is sent in the subsequent SPI_READ_OK operation.

Following an SPI_READ_REQ operation, the host must wait for a response to be ready from the device before accessing the SPI bus again. If the slave system does not assert the interrupt line within 10 ms, a HW reset or a retry from the Host is necessary. When the response is ready to be sent, the target device asserts the interrupt line to notify the host that a message is ready to be read. Only at this point is the host allowed to initiate a new SPI transaction to read back the response related to the previous write operation.

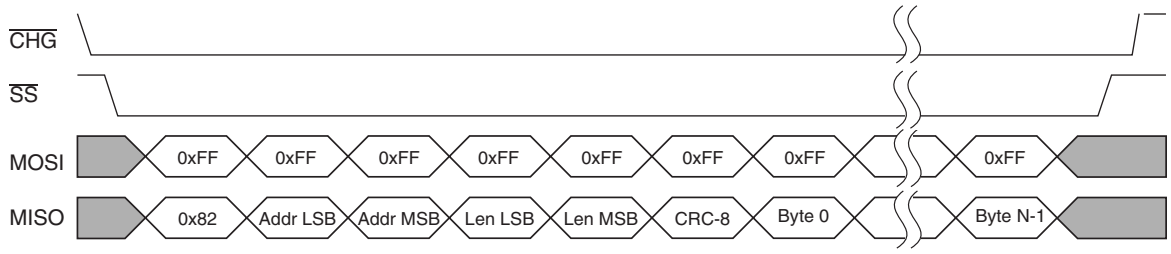
The following responses are possible following an SPI_READ_REQ operation:

- **SPI_READ_OK** – Generated if the read operation was successfully completed (the memory address and length specified by the host were within the allowed accessible memory map regions). See Section 7.4.2 “SPI_READ_OK”
- **SPI_READ_FAIL** – Generated if the read operation failed, for example if the host tries to read from an address outside the available memory map. See Section 7.4.3 “SPI_READ_FAIL”
- **SPI_INVALID_REQ** – See Section 7.5.1 “SPI_INVALID_REQ”
- **SPI_INVALID_CRC** – See Section 7.5.2 “SPI_INVALID_CRC”

7.4.2 SPI_READ_OK

Figure 7-7 shows the message format used for the read OK response.

FIGURE 7-7: SPI_READ_OK



In Figure 7-7:

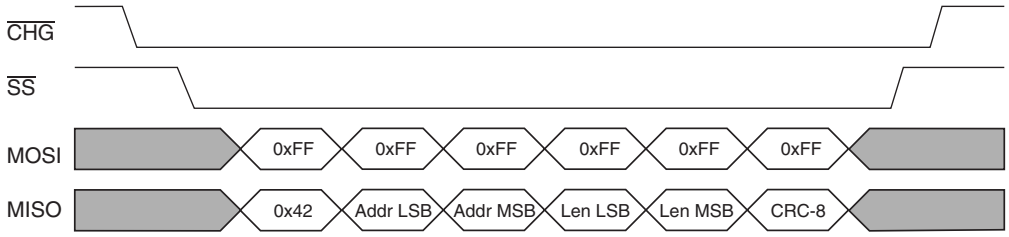
- **0x82** is the opcode
- **Addr LSB and Addr MSB** together specify the address from which the host requested the data should be read
- **Len LSB and Len MSB** together specify the length of the data in bytes. This is the total number of bytes that the Host requested to read from the slave device (excluding the header bytes)
- **CRC-8** is the 8-bit CRC
- **Byte 0 .. Byte N-1** contain the data that is to be written, where *N* the number of bytes (maximum 64 bytes)

Note that, although the slave device flushes the transmit buffer when the host performs a read operation, any attempt by the Host to read more data than expected (that is, greater than Len bytes) could cause the slave device to transmit junk data on the MISO line.

7.4.3 SPI_READ_FAIL

Figure 7-8 shows the message format used for the read fail response.

FIGURE 7-8: SPI_READ_FAIL



In Figure 7-8:

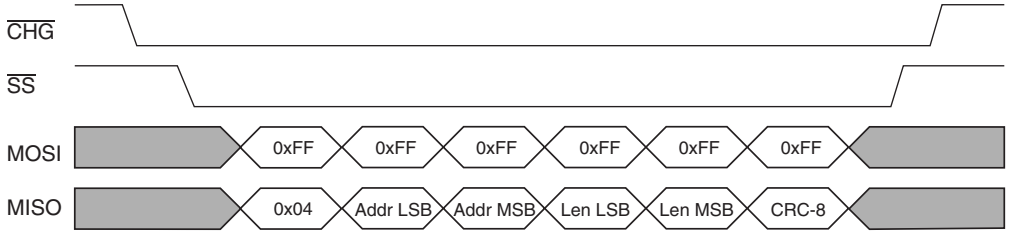
- **0x42** is the opcode
- **Addr LSB and Addr MSB** together specify the address from which the host requested the data should be read
- **Len LSB and Len MSB** together specify the length of the data in bytes. This is the total number of bytes that the Host attempted to read from the slave device (excluding the header bytes)
- **CRC-8** is the 8-bit CRC

7.5 General Operations

7.5.1 SPI_INVALID_REQ

Figure 7-9 shows the message format used for the Invalid Request response. The purpose of this opcode is to report to the host that the opcode of the last request was not recognized or that the Host has tried to perform another read or write operation without waiting for the response from the previous request.

FIGURE 7-9: SPI_INVALID_REQ



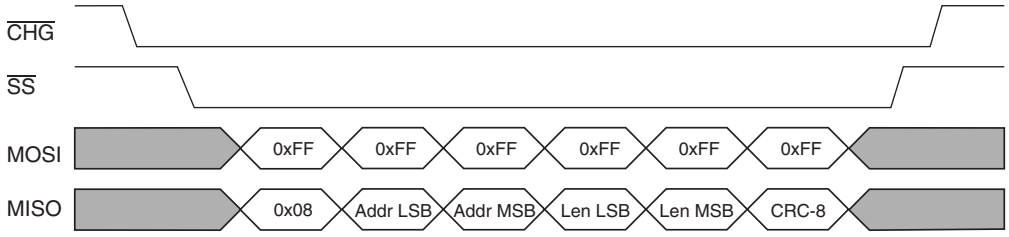
In Figure 7-9:

- **0x04** is the opcode
- **Addr LSB and Addr MSB** together specify the address received in the invalid request
- **Len LSB and Len MSB** together specify the length of the data in bytes. This is the total number of bytes that the Host attempted to read from or write to from the slave device (excluding the header bytes)
- **CRC-8** is the 8-bit CRC

7.5.2 SPI_INVALID_CRC

Figure 7-10 shows the message format used for the Invalid CRC response. The purpose of this opcode is to report an error in the CRC check performed on the received data.

FIGURE 7-10: SPI_INVALID_CRC



In Figure 7-10:

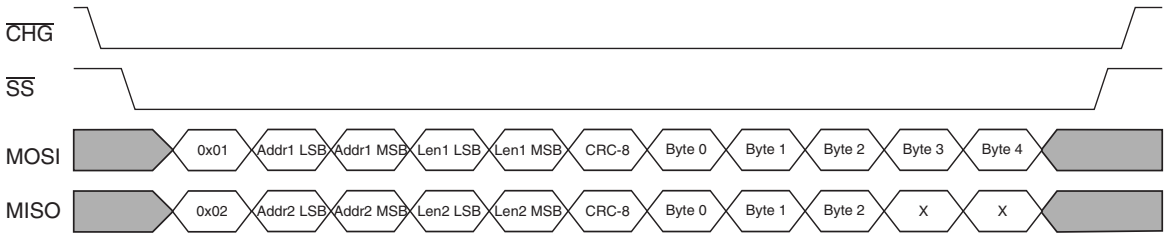
- **0x08** is the opcode
- **Addr LSB and Addr MSB** together specify the address received in the last request
- **Len LSB and Len MSB** together specify the length of the data in bytes. This is the total number of bytes that the Host attempted to read from or write to from the slave device in the last request (excluding the header bytes)
- **CRC-8** is the 8-bit CRC

7.6 Example of a Failed Transaction

In order to prevent unpredictable system behavior, the host *must* always wait for the response of the last request issued to be ready before initiating a new SPI request transaction. If the host does not comply with the protocol specification, clashes can occur.

For example, Figure 7-11 shows the situation in which an SPI_READ_OK (0x82) response with a payload of 3 bytes is expected, but the host performs an SPI_WRITE_ REQ (0x01) operation instead to write 5 bytes to address *Addr1*. In this case, the slave device outputs the SPI_READ_OK data on the MISO line (this will have been prepared in advance before the interrupt line was asserted) and ignores the new Host request received on the MOSI line. The slave device will send the Host an SPI_INVALID_REQ response, in response to the following read or write request, to indicate a violation of the SPI protocol.

FIGURE 7-11: EXAMPLE CLASH – SPI_WRITE_REQ WHEN SPI_READ_OK IS EXPECTED



8.0 PCB DESIGN CONSIDERATIONS

8.1 Introduction

The following sections give the design considerations that should be adhered to when designing a PCB layout for use with the mXT1067TD-Ax SPI Variant. Of these, power supply and ground tracking considerations are the most critical.

By observing the following design rules, and with careful preparation for the PCB layout exercise, designers will be assured of a far better chance of success and a correctly functioning product.

8.2 Printed Circuit Board

Microchip recommends the use of a four-layer printed circuit board for mXT1067TD-Ax SPI Variant applications. This, together with careful layout, will ensure that the board meets relevant EMC requirements for both noise radiation and susceptibility, as laid down by the various national and international standards agencies.

8.2.1 PCB CLEANLINESS

Modern no-clean-flux is generally compatible with capacitive sensing circuits.

CAUTION!	If a PCB is reworked to correct soldering faults relating to any device, or to any associated traces or components, be sure that you fully understand the nature of the flux used during the rework process. Leakage currents from hygroscopic ionic residues can stop capacitive sensors from functioning. If you have any doubts, a thorough cleaning after rework may be the only safe option.

8.3 Power Supply

8.3.1 SUPPLY QUALITY

While the device has good Power Supply Rejection Ratio properties, poorly regulated and/or noisy power supplies can significantly reduce performance.

Particular care should be taken of the AVdd supply, as it supplies the sensitive analog stages in the device.

8.3.2 SUPPLY RAILS AND GROUND TRACKING

Power supply and clock distribution are the most critical parts of any board layout. Because of this, it is advisable that these be completed before any other tracking is undertaken. After these, supply decoupling, and analog and high speed digital signals should be addressed. Track widths for all signals, especially power rails should be kept as wide as possible in order to reduce inductance.

The Power and Ground planes themselves can form a useful capacitor. Flood filling for either or both of these supply rails, therefore, should be used where possible. It is important to ensure that there are no floating copper areas remaining on the board: all such areas should be connected to the ground plane. The flood filling should be done on the outside layers of the board.

8.3.3 POWER SUPPLY DECOUPLING

Decoupling capacitors should be fitted as specified in Section 2.2 “Schematic Notes”.

The decoupling capacitors must be placed as close as possible to the pin being decoupled. The traces from these capacitors to the respective device pins should be wide and take a straight route. They should be routed over a ground plane as much as possible. The capacitor ground pins should also be connected directly to a ground plane.

Surface mounting capacitors are preferred over wire-leaded types due to their lower ESR and ESL. It is often possible to fit these decoupling capacitors underneath and on the opposite side of the PCB to the digital ICs. This will provide the shortest tracking, and most effective decoupling possible.

8.3.4 VOLTAGE PUMP

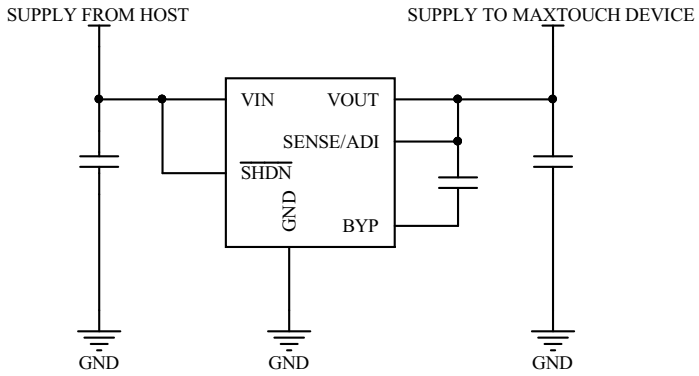
The traces for the voltage pump capacitor between EXTCAP2 and EXTCAP3 (Cd on the schematic in Section 2.0 “Schematic”) should be kept as short and as wide as possible for best pump performance. They should also be routed as parallel and as close as possible to each other in order to reduce emissions, and ideally the traces should be the same length.

8.3.5 VOLTAGE REGULATORS

Each supply rail requires a Low Drop-Out (LDO) voltage regulator, although an LDO can be shared where supply rails share the same voltage level.

Figure 8-1 shows an example circuit for an LDO.

FIGURE 8-1: EXAMPLE LDO CIRCUIT



An LDO regulator should be chosen that provides adequate output capability, low noise, good load regulation and step response. The voltage regulators listed in Table 8-1 have been tested and found to work well with maXTouch devices. If it is desired to use an alternative LDO, however, certain performance criteria should be verified before using the device. These are:

- Stable with high value multi-layer ceramic capacitors on the output
- Low output noise – ideally less than 100 μV_{RMS} over the range 10 Hz to 1 MHz
- Good load transient response – this should be less than 35 mV peak when a load step change of 100 mA is applied at the device output terminal
- No-load stable – Some LDOs become unstable if the output current falls below a certain minimum. If this is the case, then this minimum must be lower than the minimum current consumed by the mXT1067TD-Ax SPI Variant (for example, in deep sleep).

TABLE 8-1: SUITABLE LDO REGULATORS

Manufacturer	Device	Current Rating (mA)
Microchip Technology Inc.	MCP1824	300
Microchip Technology Inc.	MCP1824S	300
Microchip Technology Inc.	MAQ5300	300
Microchip Technology Inc.	MCP1725	500
Analog Devices	ADP122/ADP123	300
Diodes Inc.	AP2125	300
Diodes Inc.	AP7335	300
Linear Technology	LT1763CS8-3.3	500
NXP	LD6836	300
Texas Instruments	LP3981	300

Note: Some manufacturers claim that minimal or no capacitance is required for correct regulator operation. However, in all cases, a minimum of a 1.0 µF ceramic, low ESR capacitor at the input and output of these devices should be used. The manufacturer's datasheets should always be referred to when selecting capacitors for these devices and the typical recommended values, types and dielectrics adhered to.

8.3.6 SINGLE SUPPLY OPERATION

When designing a PCB for an application using a single LDO, extra care should be taken to ensure short, low inductance traces between the supply and the touch controller supply input pins. Ideally, tracking for the individual supplies should be arranged in a star configuration, with the LDO at the junction of the star. This will ensure that supply current variations or noise in one supply rail will have minimum effect on the other supplies. In applications where a ground plane is not practical, this same star layout should also apply to the power supply ground returns.

Only regulators with a 300 mA or greater rating can be used in a single-supply design.

Refer to the following application note for more information:

- Application Note: MXTAN0208 – *Design Guide for PCB Layouts for maXTouch Touch Controllers*

8.3.7 MULTIPLE VOLTAGE REGULATOR SUPPLY

The AVdd supply stability is critical for the device because this supply interacts directly with the analog front end. If noise problems exist when using a single LDO regulator, Microchip recommends that AVdd is supplied by a regulator that is separate from the digital supply. This reduces the amount of noise injected into the sensitive, low signal level parts of the design.

8.4 Driven Shield Line

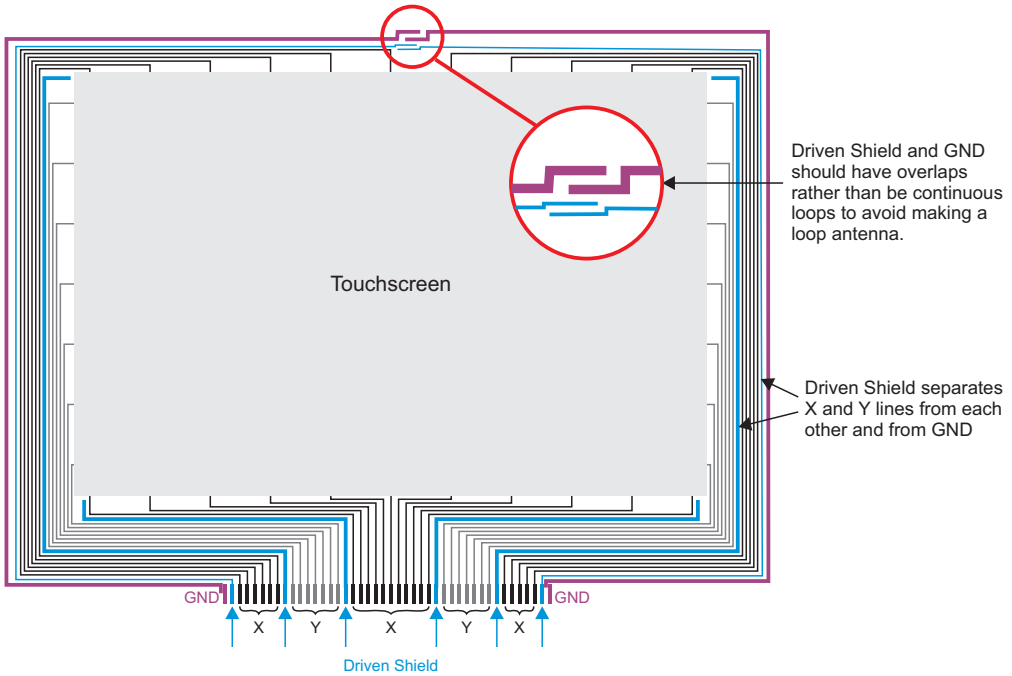
The driven shield line can be used to provide a guard track that serves as Ground in mutual capacitance operation and as a driven shield in self capacitance operation.

The guard track must be routed between the X and Y tracks, as well as between the X/Y tracks and Ground. It should be fairly wide to avoid X-to-Y coupling in mutual capacitance operation, as the guard track will act as Ground in this circumstance.

A guard track is also needed between any self capacitance X/Y lines and mutual capacitance only X/Y lines (for example, between Multiple Touch Touchscreen T100 and Key Array T15 lines).

NOTE	DS0 is internally multiplexed to X31. X31 must be configured for use if DS0 is to be used (either as a driven shield for self capacitance measurements or as a Ground guard track in a mutual capacitance only design), otherwise DS0 cannot be used in the user's design.

FIGURE 8-2: EXAMPLE DRIVEN SHIELD ROUTING



NOTE: Sample touchscreen for illustrative purposes only. The number of X/Y lines available on any given device might differ from that shown here. Similarly, the routing of the X/Y lines shown should not be taken as indicative of any preferred layout and the user's layout may vary.

8.5 ESD Ground Routing

To avoid damage due to ESD strikes, the outermost track on the sensor should be an ESD ground (see Figure 8-2). Like the driven shield, this should completely surround the sensor but with an overlap at the top rather than forming a complete loop.

To avoid electromagnetic induction of currents into the driven shield trace, a minimum separation of 0.3 mm should be maintained between the ESD GND trace and the Driven Shield.

The ESD ground traces should be connected to a dedicated ground trace in the PCB, and routed such that ESD strike currents do not flow under or close to the touch controller or the connecting wiring between it and the touchscreen array. The ESD ground should be connected in to the main system ground at a star point at the main GND connection to the PCB.

See also:

- MXTAN0208 – *Design guide for PCB Layouts for maXTouch Touch Controllers*

8.6 Analog I/O

In general, tracking for the analog I/O signals from the device should be kept as short as possible. These normally go to a connector which interfaces directly to the touchscreen.

Ensure that adequate ground-planes are used. An analog ground plane should be used in addition to a digital one. Care should be taken to ensure that both ground planes are kept separate and are connected together only at the point of entry for the power to the PCB. This is usually at the input connector.

8.7 Component Placement and Tracking

It is important to orient all devices so that the tracking for important signals (such as power and clocks) are kept as short as possible.

8.7.1 DIGITAL SIGNALS

In general, when tracking digital signals, it is advisable to avoid sharp directional changes on sensitive signal tracks (such as analog I/O) and any clock or crystal tracking.

A good ground return path for all signals should be provided, where possible, to ensure that there are no discontinuities.

8.8 EMC and Other Observations

The following recommendations are not mandatory, but may help in situations where particularly difficult EMC or other problems are present:

- Try to keep as many signals as possible on the inside layers of the board. If suitable ground flood fills are used on the top and bottom layers, these will provide a good level of screening for noisy signals, both into and out of the PCB.
- Ensure that the on-board regulators have sufficient tracking around and underneath the devices to act as a heatsink. This heatsink will normally be connected to the 0 V or ground supply pin. Increasing the width of the copper tracking to any of the device pins will aid in removing heat. There should be no solder mask over the copper track underneath the body of the regulators.
- Ensure that the decoupling capacitors, especially high capacity ceramic type, have the requisite low ESR, ESL and good stability/temperature properties. Refer to the regulator manufacturer’s datasheet for more information.

9.0 GETTING STARTED WITH MXT1067TD-AT/MXT1067TD-AB SPI VARIANT

9.1 Establishing Contact

9.1.1 COMMUNICATION WITH THE HOST

The host can use the following interface to communicate with the device:

- SPI interface (see Section 7.0 “SPI Communications”)

9.1.2 POWER-UP SEQUENCE

On power-up, the $\overline{\text{CHG}}$ line goes low to indicate that there is new data to be read from the device. If the $\overline{\text{CHG}}$ line does not go low, there is a problem with the device.

Once the $\overline{\text{CHG}}$ line goes low, the host should attempt to read the first 7 bytes of memory from location 0x00 to establish that the device is present and running following power-up.

A checksum check is performed on the configuration settings held in the non-volatile memory. If the checksum does not match a stored copy of the last checksum, then this indicates that the settings have become corrupted. The host should write a correct configuration to the device if the read checksum does not match the expected checksum, or if the configuration error bit in the message data from the Command Processor T6 object is set.

9.2 Using the Object Protocol

The device has an object-based protocol that is used to communicate with the device. Typical communication includes configuring the device, sending commands to the device, and receiving messages from the device.

The host must perform the following initialization so that it can communicate with the device:

1. Read the start positions of all the objects in the device from the Object Table and build up a list of these addresses.
2. Use the Object Table to calculate the report IDs so that messages from the device can be correctly interpreted.

9.2.1 CLASSES OF OBJECTS

The mXT1067TD-Ax SPI Variant contains the following classes of objects:

- **Debug objects** – provide a raw data output method for development and testing.
- **General objects** – required for global configuration, transmitting messages and receiving commands.
- **Touch objects** – operate on measured signals from the touch sensor and report touch data.
- **Signal processing objects** – process data from other objects (typically signal filtering operations).
- **Support objects** – provide additional functionality on the device.

9.2.2 OBJECT INSTANCES

TABLE 9-1: OBJECTS ON THE MXT1067TD-Ax SPI VARIANT

Object	Description	Number of Instances	Usage
Debug Objects			
Diagnostic Debug T37	Allows access to diagnostic debug data to aid development.	1	Debug commands only. No configuration/tuning necessary. Not for use in production.
General Objects			
Message Processor T5	Handles the transmission of messages. This object holds a message in its memory space for the host to read.	1	No configuration necessary.
Command Processor T6	Performs a command when written to. Commands include reset, calibrate and backup settings.	1	No configuration necessary.

TABLE 9-1: OBJECTS ON THE MXT1067TD-Ax SPI VARIANT (CONTINUED)

Object	Description	Number of Instances	Usage
Power Configuration T7	Controls the sleep mode of the device. Power consumption can be lowered by controlling the acquisition frequency and the sleep time between acquisitions.	1	Must be configured before use.
Acquisition Configuration T8	Controls how the device takes each capacitive measurement.	1	Must be configured before use.
Touch Objects			
Key Array T15	Defines a rectangular array of keys. A Key Array T15 object reports simple on/off touch information.	1	Enable and configure as required.
Multiple Touch Touchscreen T100	Creates a Touchscreen that supports the tracking of more than one touch.	1	Enable and configure as required.
Signal Processing Objects			
Key Thresholds T14	Allows different thresholds to be specified for each key in a Key Array.	1	Configure as required.
Touch Suppression T42	Suppresses false detections caused by unintentional large touches by the user.	1	Enable and configure as required.
Shieldless T56	Allows a sensor to use true single-layer co-planar construction.	1	Enable and configure as required.
Lens Bending T65	Compensates for lens deformation (lens bending) by attempting to eliminate the disturbance signal from the reported deltas.	3	Enable and configure as required.
Noise Suppression T72	Performs various noise reduction techniques during sensor signal acquisition.	1	Enable and configure as required.
Glove Detection T78	Allows for the reporting of glove touches.	1	Enable and configure as required.
Retransmission Compensation T80	Limits the negative effects on touch signals caused by poor device coupling to ground or moisture on the sensor.	1	Enable and configure as required.
Self Capacitance Noise Suppression T108	Suppresses the effects of external noise within the context of self capacitance touch measurements.	1	Enable and configure as required.
Self Capacitance Grip Suppression T112	Allows touches to be reported from the self capacitance measurements while the device is being gripped.	1	Enable and configure as required.
Support Objects			
Communications Configuration T18	Configures additional communications behavior for the device.	1	Check and configure as necessary.
GPIO Configuration T19	Allows the host controller to configure and use the general purpose I/O pins on the device.	1	Enable and configure as required.
Self Test T25	Configures and performs self-test routines to find faults on a touch sensor.	1	Configure as required for pin test commands.
User Data T38	Provides a data storage area for user data.	1	Configure as required.
Message Count T44	Provides a count of pending messages.	1	Read-only object.
CTE Configuration T46	Controls the capacitive touch engine for the device.	1	Must be configured.
Timer T61	Provides control of a timer.	6	Enable and configure as required.

TABLE 9-1: OBJECTS ON THE MXT1067TD-Ax SPI VARIANT (CONTINUED)

Object	Description	Number of Instances	Usage
Dynamic Configuration Controller T70	Allows rules to be defined that respond to system events.	20	Enable and configure as required.
Dynamic Configuration Container T71	Allows the storage of user configuration on the device that can be selected at runtime based on rules defined in the Dynamic Configuration Controller T70 object.	1	Configure if Dynamic Configuration Controller T70 is in use.
Touch Event Trigger T79	Configures touch triggers for use with the event handler.	3	Enable and configure as required.
Auxiliary Touch Configuration T104	Allows the setting of self capacitance gain and thresholds for a particular measurement to generate auxiliary touch data for use by other objects.	1	Enable and configure if using self capacitance measurements
Self Capacitance Global Configuration T109	Provides configuration for self capacitance measurements employed on the device.	1	Check and configure as required (if using self capacitance measurements).
Self Capacitance Tuning Parameters T110	Provides configuration space for a generic set of settings for self capacitance measurements.	6	Use under the guidance of Microchip field engineers only.
Self Capacitance Configuration T111	Provides configuration for self capacitance measurements employed on the device.	2	Check and configure as required (if using self capacitance measurements).
Self Capacitance Measurement Configuration T113	Configures self capacitance measurements to generate data for use by other objects.	1	Enable and configure as required.
Self Capacitance Voltage Modulation T133	Controls the voltage modulation on self capacitance scans.	2	Enable and configure as required.

9.2.3 CONFIGURING AND TUNING THE DEVICE

The objects are designed such that a default value of zero in their fields is a “safe” value that typically disables functionality. The objects must be configured before use and the settings written to the non-volatile memory using the Command Processor T6 object.

Perform the following actions for each object:

1. Enable the object, if the object requires it.
2. Configure the fields in the object, as required.
3. Enable reporting, if the object supports messages, to receive messages from the object.

9.3 Writing to the Device

The following mechanism can be used to write to the device:

- Using the SPI write operation (see Section 7.3 “Write Operation and Responses”).

Communication with the device is achieved by writing to the appropriate object:

- To send a command to the device, an appropriate command is written to the Command Processor T6 object.
- To configure the device, a configuration parameter is written to the appropriate object. For example, writing to the Power Configuration T7 configures the power consumption for the device and writing to the touchscreen Multiple Touch Touchscreen T100 object sets up the touchscreen. Some objects are optional and need to be enabled before use.

IMPORTANT!	When the host issues any command within an object that results in a flash write to the device Non-Volatile Memory (NVM), that object should have its CTRL RPTEN bit set to 1, if it has one. This ensures that a message from the object writing to the NVM is generated at the completion of the process and an assertion of the CHG line is executed. The host must also ensure that the assertion of the CHG line refers to the expected object report ID before asserting the RESET line to perform a reset. Failure to follow this guidance may result in a corruption of device configuration area and the generation of a CFGERR.

9.4 Reading from the Device

Status information is stored in the Message Processor T5 object. This object can be read to receive any status information from the device. The following mechanism provides an interrupt-style interface for reading messages in the Message Processor T5 object:

- The CHG line is asserted whenever a new message is available in the Message Processor T5 object (see Section 7.2.1 “Change Line (CHG)”). See Section 7.4 “Read Operation and Responses” for information on the format of the SPI read operation.

  When using the SPI interface, two SPI transactions must take place: the first is an SPI Read request which is used to set the address pointer (Address LSByte and MSByte) and to indicate to the slave device how many bytes (Length LSByte and MSByte) the Host wants to read; the second is a response which comes with a payload that actually contains the data that was requested (see Section 7.4 “Read Operation and Responses”).

Note that the host should always wait to be notified of messages; the host should not poll the device for messages. In particular, the CHG line must never be polled. The reason for this is that when polling the Host handling of the CHG line will be level based instead of falling edge based, as is required.

10.0 DEBUGGING AND TUNING

10.1 SPI Debug Interface

The SPI Debug Interface is used for tuning and debugging when running the system and allows the development engineer to use Microchip maXTouch Studio to read the real-time raw data. This uses the low-level debug port.

The SPI Debug Interface consists of the $\overline{\text{DBG\_SS}}$, DBG_CLK, and DBG_DATA lines. It is recommended that these pins are routed to test points on all designs such that they can be connected to external hardware during system development. These lines should not be connected to power or GND. See Section 2.2.9 “SPI Debug Interface” for more details.

The SPI Debug Interface is enabled by the Command Processor T6 object and by default will be off.

NOTE	The touch controller will take care of the pin configuration. When the $\overline{\text{DBG\_SS}}$, DBG_CLK, and DBG_DATA lines are in use for debugging, any alternative function for the pins cannot be used.

10.2 Object-based Protocol

The device provides a mechanism for obtaining debug data for development and testing purposes by reading data from the Diagnostic Debug T37 object.

NOTE	The Diagnostic Debug T37 object is of most use for simple tuning purposes. When debugging a design, it is preferable to use the SPI Debug Interface, as this will have a much higher bandwidth and can provide real-time data.

10.3 Self Test

There is a Self Test T25 object that runs self-test routines in the device to find hardware faults on the sense lines and the electrodes. This object also performs an initial pin fault test on power-up to ensure that there is no pin short (X-to-Y, or sense pin to power or GND) before the high-voltage supply is enabled inside the chip. A high-voltage short on the sense lines could damage the device.

In addition to one-off hardware tests, the Self Test T25 object can also provide continuous monitoring of the health of the device while it is in operation. A periodic test can be run at a user-specified interval and reports pass and/or fail messages (as determined by the device configuration). Reporting is achieved either by standard Self Test T25 object protocol messages or by a dedicated hardware GPIO pin, configured using the GPIO Configuration T19 object.

11.0 SPECIFICATIONS

11.1 Absolute Maximum Specifications

Vdd	3.6V
VddIO	3.6V
AVdd	3.6V
Maximum continuous combined pin current, all GPIO*n* pins	60 mA
Voltage forced onto any pin	–0.3 V to Vdd/VddIO/AVdd + 0.3 V
Configuration parameters maximum writes	10,000
Maximum junction temperature	125°C

CAUTION! Stresses beyond those listed under *Absolute Maximum Specifications* may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum specification conditions for extended periods may affect device reliability.

11.2 Recommended Operating Conditions

Operating temperature	mXT1067TD-AT: –40°C to +85°C (Grade 3)
	mXT1067TD-AB: –40°C to +105°C (Grade 2)
Storage temperature	–60°C to +150°C
Vdd	3.3 V ±5%
VddIO	3.3 V ±5%
AVdd	3.3 V ±5%
XVdd with internal voltage doubler enabled	2 × Vdd
XVdd with internal voltage doubler disabled	Connected to Vdd (3.3 V ±5%)
Temperature slew rate	10°C/min

11.2.1 DC CHARACTERISTICS

11.2.1.1 Analog Voltage Supply – AVdd

Parameter	Min	Typ	Max	Units	Notes
AVdd					
Operating limits	3.14	3.3	3.47	V	
Supply Rise Rate	–	–	0.036	V/µs	For example, for a 3.3 V rail, the voltage should take a minimum of 92 µs to rise

11.2.1.2 Digital Voltage Supply – VddIO, Vdd

Parameter	Min	Typ	Max	Units	Notes
VddIO					
Operating limits	3.14	3.3	3.47	V	
Supply Rise Rate	–	–	0.036	V/µs	For example, for a 3.3 V rail, the voltage should take a minimum of 92 µs to rise
Vdd					
Operating limits	3.14	3.3	3.47	V	
Supply Rise Rate	–	–	0.036	V/µs	For example, for a 3.3 V rail, the voltage should take a minimum of 92 µs to rise
Supply Fall Rate	–	–	0.05	V/µs	For example, for a 3.3 V rail, the voltage should take a minimum of 66 µs to fall

11.2.1.3 XVdd Voltage Supply – XVdd

Parameter	Min	Typ	Max	Units	Notes
XVdd					
Operating limits – voltage doubler enabled	–	2 × Vdd	–	V	
Operating limits – voltage doubler disabled	–	Vdd	–	V	

11.2.2 POWER SUPPLY RIPPLE AND NOISE

Parameter	Min	Typ	Max	Units	Notes
Vdd	–	–	±50	mV	Across frequency range 1 Hz to 1 MHz
AVdd	–	–	±40	mV	Across frequency range 1 Hz to 1 MHz, with Noise Suppression enabled

11.3 Test Configuration

The configuration values listed below were used in the reference unit to validate the interfaces and derive the characterization data provided in the following sections.

TABLE 11-1: TEST CONFIGURATION

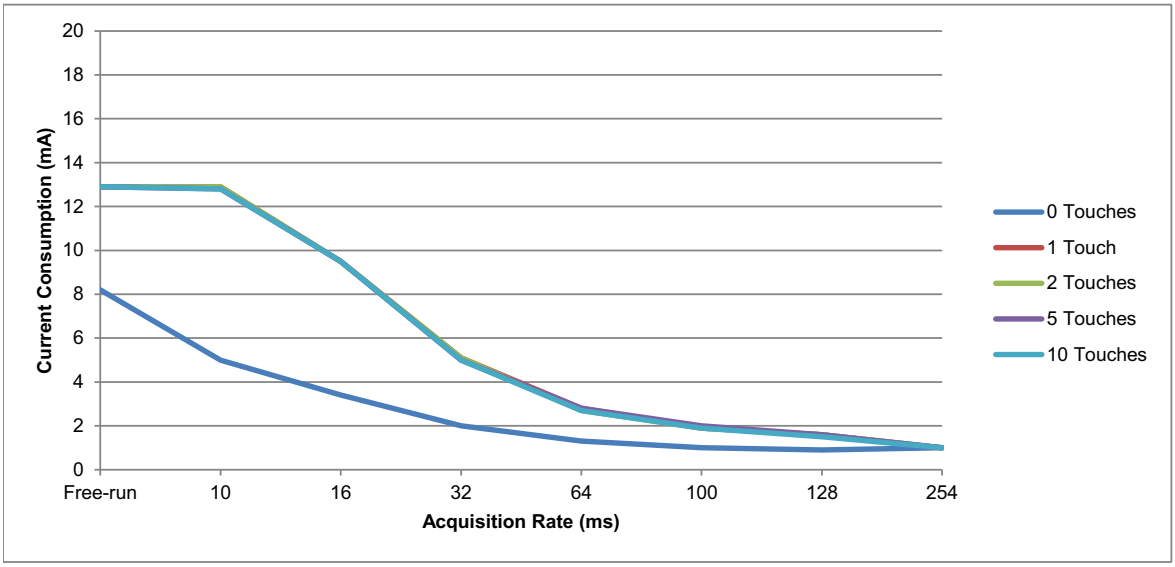
Object/Parameter	Description/Setting (Numbers in Decimal)
Acquisition Configuration T8	
CHRGTIME	39
MEASALLOW	3
Self Test T25	Object Enabled
Touch Suppression T42	Object Enabled
CTE Configuration T46	
IDLESYNCSPERX	16
ACTVSYNCSPERX	16
Shieldless T56	Object Enabled
INTTIME	21
Lens Bending T65 Instance 0	Object Instance Enabled
Lens Bending T65 Instance 1	Object Instance Enabled
Lens Bending T65 Instance 2	Object Instance Enabled
Noise Suppression T72	Object Enabled
Glove Detection T78	Object Enabled
Retransmission Compensation T80	Object Enabled
Multiple Touch Touchscreen T100	Object Enabled
XSIZE	41
YSIZE	26
Auxiliary Touch Configuration T104	Object Enabled
Self Capacitance Noise Suppression T108	Object Enabled
Self Capacitance Configuration T111 Instance 0	
INTTIME	65
IDLESYNCSPERL	24
ACTVSYNCSPERL	24
Self Capacitance Configuration T111 Instance 1	
INTTIME	65
IDLESYNCSPERL	32
ACTVSYNCSPERL	32
Self Capacitance Voltage Modulation T133 Instance 0	Object Instance Enabled
Self Capacitance Voltage Modulation T133 Instance 1	Object Instance Enabled

11.4 Current Consumption

NOTE The characterization charts show typical values based on the configuration in Table 11-1. Actual power consumption in the user's application will depend on the circumstances of that particular project and will vary from that shown here. Further tuning will be required to achieve an optimal performance.

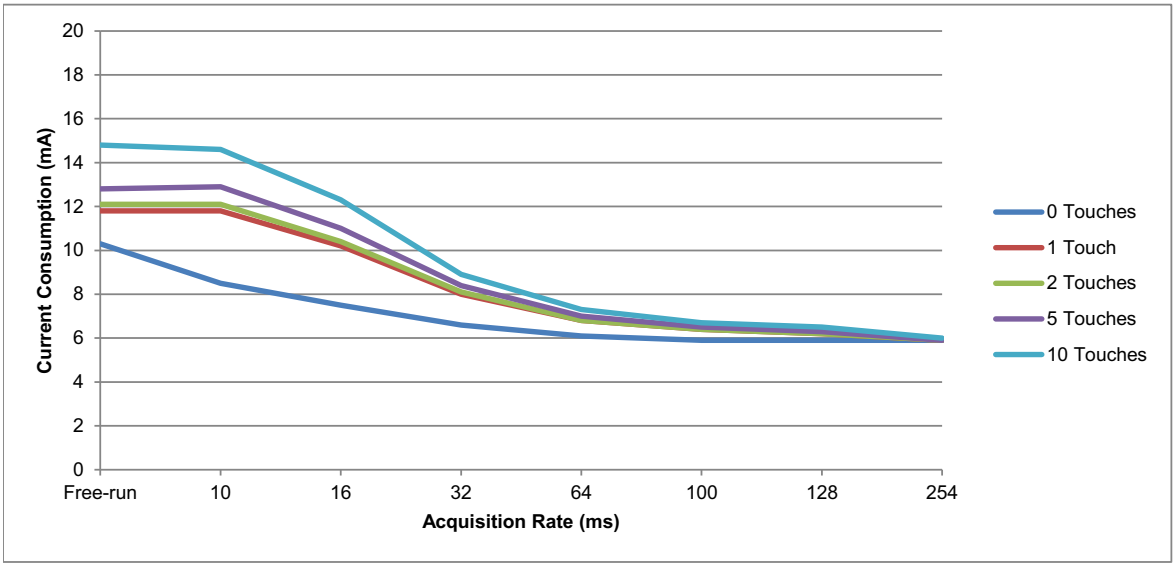
11.4.1 AVDD 3.3V

	Current Consumption (mA)				
Acquisition Rate (ms)	**0 Touches**	**1 Touch**	**2 Touches**	**5 Touches**	**10 Touches**
Free-run	8.2	12.9	12.9	12.9	12.9
10	5	12.9	12.9	12.8	12.8
16	3.4	9.5	9.5	9.5	9.5
32	2	5.1	5.1	5	5
64	1.3	2.8	2.7	2.8	2.7
100	1	1.9	1.9	2	1.9
128	0.9	1.6	1.6	1.6	1.5
254	1	1	1	1	1



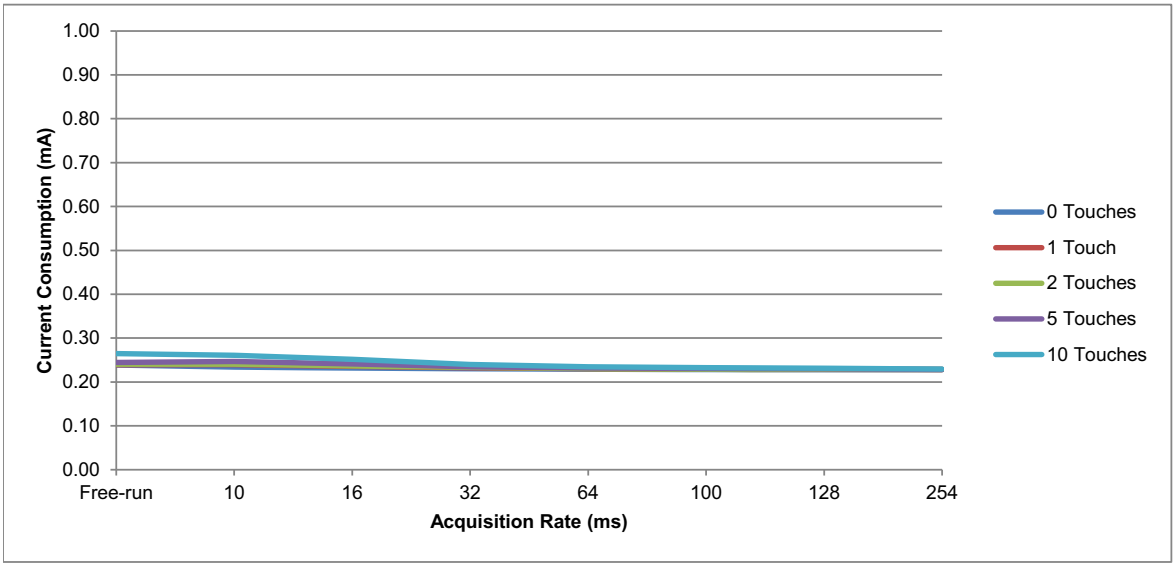
11.4.2 VDD 3.3V

	Current Consumption (mA)				
Acquisition Rate (ms)	**0 Touches**	**1 Touch**	**2 Touches**	**5 Touches**	**10 Touches**
Free-run	10.3	11.8	12.1	12.8	14.8
10	8.5	11.8	12.1	12.9	14.6
16	7.5	10.2	10.4	11	12.3
32	6.6	8	8.1	8.4	8.9
64	6.1	6.8	6.8	7	7.3
100	5.9	6.4	6.4	6.5	6.7
128	5.9	6.2	6.2	6.3	6.5
254	5.9	5.9	5.9	5.9	6



11.4.3 VDDIO 3.3V

	Current Consumption (mA)				
Acquisition Rate (ms)	**0 Touches**	**1 Touch**	**2 Touches**	**5 Touches**	**10 Touches**
Free-run	0.24	0.24	0.24	0.24	0.26
10	0.23	0.24	0.24	0.25	0.26
16	0.23	0.24	0.24	0.24	0.25
32	0.23	0.23	0.23	0.23	0.24
64	0.23	0.23	0.23	0.23	0.23
100	0.23	0.23	0.23	0.23	0.23
128	0.23	0.23	0.23	0.23	0.23
254	0.23	0.23	0.23	0.23	0.23



11.4.4 DEEP SLEEP

T_A = 25°C

Parameter	Min	Typ	Max	Units	Notes
Deep Sleep Current	–	6	–	mA	Vdd = 3.3 V, AVdd = 3.3 V, VddIO = 3.3V
Deep Sleep Power	–	20	–	mW	Vdd = 3.3 V, AVdd = 3.3 V, VddIO = 3.3V

11.5 Timing Specifications

NOTE The figures below show typical values based on the test configuration. Actual timings in the user's application will depend on the circumstances of that particular project and will vary from those shown below. Further tuning will be required to achieve an optimal performance.

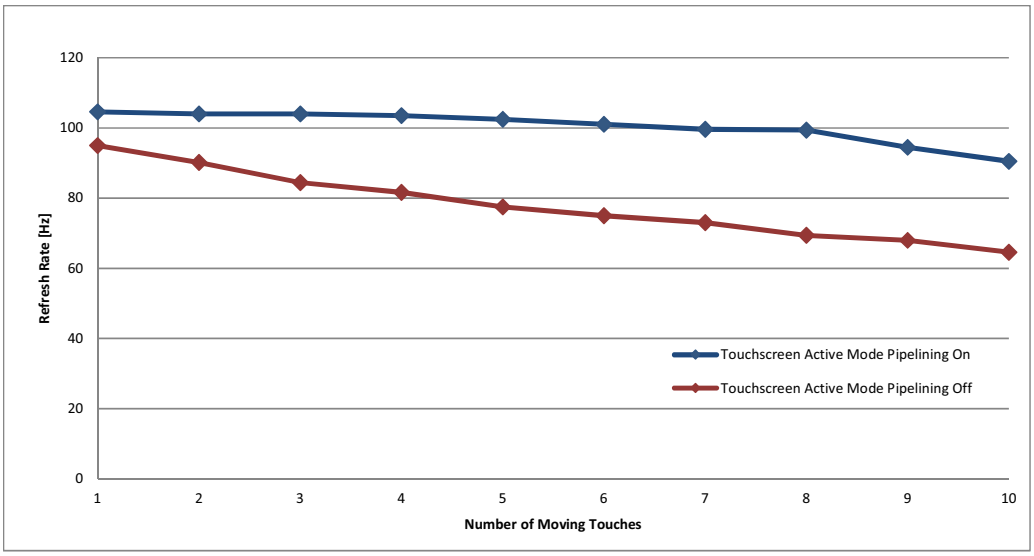
11.5.1 TOUCH LATENCY

Conditions: XSIZE = 41; YSIZE = 26; CHRGTIME = 39; IDLESYNCSPERX = 16; ACTVSYNCSPERX = 16;
Idle Primary = Self Capacitance; Active Primary = Mutual Capacitance; IDLEACQINT = ACTVACQINT = Free Run
T = ambient temperature; Finger center of screen; Reporting off (except T100); C_{pk} Process Capability Index calculation not applied

T100 TCHDIDOWN	Pipelining Off			Pipelining On			Units
	Min	Typ	Max	Min	Typ	Max	
2	22.1	27.3	36.4	19.7	21.9	34.8	ms
1	8.0	14.7	22.4	5.4	10.8	18.0	ms
0	8.4	14.7	22.3	5.7	11.9	17.7	ms
Disabled (DISTCHDIDOWN = 1)	7.8	10.7	20.1	5.5	10.6	18.2	ms

11.5.2 REPORT RATE

Conditions: XSIZE = 41, YSIZE = 26; CHRGTIME = 39; IDLESYNCSPERX = 16, ACTVSYNCSPERX = 16; T = ambient temperature



11.5.3 BURST FREQUENCY TOLERANCE

The burst frequency is directly correlated to the system clock. The burst frequency tolerance depends on the tolerance of the system's oscillator (see Table 11-2).

TABLE 11-2: OSCILLATOR TOLERANCE

Conditions: T= –40°C, 25°C, 85°C, 105°C

Min Drift	Nominal	Max Drift	Notes
–5%	53 MHz (calibrated)	+5%	Minimum/Maximum drift over temperature is specified as percentage below/above nominal frequency

11.5.4 RESET TIMINGS

Parameter	Min	Typ	Max	Units	Notes
Power on to $\overline{\text{CHG}}$ line low	–	95	–	ms	Vdd supply for POR VddIO supply for external reset
Hardware reset to $\overline{\text{CHG}}$ line low	–	95	–	ms	
Software reset to $\overline{\text{CHG}}$ line low	–	112	–	ms	

Note 1: Any $\overline{\text{CHG}}$ line activity before the power-on or reset period has expired should be ignored by the host. Operation of this signal cannot be guaranteed before the power-on/reset periods have expired.

11.6 Touch Accuracy and Repeatability

Parameter	Min	Typ	Max	Units	Notes
Linearity	–	±0.5	–	mm	Finger diameter 8 mm
Accuracy (across all areas of screen)	–	0.5	–	mm	Finger diameter 8 mm
Repeatability	–	±0.25	–	%	X axis with 12-bit resolution

11.7 Touchscreen Sensor Characteristics

Parameter	Description	Value
Cm	Mutual capacitance	Typical value is between 0.15 pF and 10 pF on a single node.
Cpx	Mutual capacitance load to X	Microchip recommends a maximum load of 300 pF on each X or Y line. (1)
	With Internal Voltage Pump	Maximum recommended load on each X line: (2) Cpx + (*num_Y* × Cm) < 125 pF
	With Internal Voltage Pump and Dual X	Maximum recommended load on each X line: (2) Cpx + (2 × *num_Y* × Cm) < 125 pF
Cpy	Mutual capacitance load to Y	Microchip recommends a maximum load of 300 pF on each X or Y line. (1)
Cpx	Self capacitance load to X	Microchip recommends a maximum load of 100 pF on each X or Y line. (1)
Cpy	Self capacitance load to Y	
ΔCpx	Self capacitance imbalance on X	Nominal value is 20.9 pF. Value increases by 1 pF for every 45 pF reduction in Cpx/Cpy (based on 100 pF load)
ΔCpy	Self capacitance imbalance on Y	
Cpds0	Self capacitance load to Driven Shield	Microchip recommends a maximum load of 100 pF on the Driven Shield line. (1)

Note 1: Please contact your Microchip representative for advice if you intend to use higher values.
2: *num_Y* = Number of active Y lines defined by Multiple Touch Touchscreen T100.

11.8 Input/Output Characteristics

Parameter	Description	Min	Typ	Max	Units	Notes
Input (GPIO*n*, FSYNC, PSYNC, MOSI, SCK, MISO, $\overline{\text{CHG}}$)						
Vil	Low input logic level	–0.3	–	0.3 × VddIO	V	
Vih	High input logic level	0.7 × VddIO	–	VddIO	V	
Iil	Input leakage current	–	–	1	µA	Pull-up resistors disabled
$\overline{\text{RESET}}$	Internal pull-up resistor	20	40	60	kΩ	
GPIOs	Internal pull-up/pull-down resistor					

Parameter	Description	Min	Typ	Max	Units	Notes
Output (GPIO*n*, MOSI, SCK, $\overline{\text{CHG}}$, DBG_CLK, DBG_DATA, $\overline{\text{DBG\_SS}}$)						
Vol	Low output voltage	0	–	0.2 × VddIO	V	Iol = –4 mA
Voh	High output voltage	0.8 × VddIO	–	VddIO	V	Ioh = 4 mA

11.9 SPI Bus Specification

Parameter	Specification
Mode	Mode 3 (CPOL = 1 and CPHA = 1)
Clock idle state	High
Setup on	Leading (falling) edge
Sample on	Trailing (rising) edge
Word size	8-bit
Maximum clock frequency	8 MHz

11.10 Thermal Packaging

11.10.1 THERMAL DATA

Parameter	Description	Typ	Unit	Condition	Package
θ_{JA}	Junction to ambient thermal resistance	45.4	°C/W	Still air	128-lead TQFP 14 × 14 × 1 mm
θ_{JC}	Junction to case thermal resistance	7.9	°C/W		128-lead TQFP 14 × 14 × 1 mm

11.10.2 JUNCTION TEMPERATURE

The maximum junction temperature allowed on this device is 125°C.

The average junction temperature in °C (T_J) for this device can be obtained from the following:

$$T_J = T_A + (P_D \times \theta_{JA})$$

If a cooling device is required, use this equation:

$$T_J = T_A + (P_D \times (\theta_{HEATSINK} + \theta_{JC}))$$

where:

- θ_{JA}= package thermal resistance, Junction to ambient (°C/W) (see Section 11.10.1 “Thermal Data”)
- θ_{JC} = package thermal resistance, Junction to case thermal resistance (°C/W) (see Section 11.10.1 “Thermal Data”)
- $\theta_{HEATSINK}$ = cooling device thermal resistance (°C/W), provided in the cooling device datasheet
- P_D = device power consumption (W)
- T_A is the ambient temperature (°C)

11.11 ESD Information

Parameter	Value	Reference standard	Notes
Human Body Model (HBM)	±2000 V	AEC–Q100	
Charge Device Model (CDM)	±500 V	AEC–Q100	Except corner pins
	±750 V	AEC–Q100	Corner pins only

11.12 Soldering Profile

Profile Feature	Green Package
Average Ramp-up Rate (217°C to Peak)	3°C/s max
Preheat Temperature 175°C ±25°C	150 – 200°C
Time Maintained Above 217°C	60 – 150 s
Time within 5°C of Actual Peak Temperature	30 s
Peak Temperature Range	260°C
Ramp down Rate	6°C/s max
Time 25°C to Peak Temperature	8 minutes max

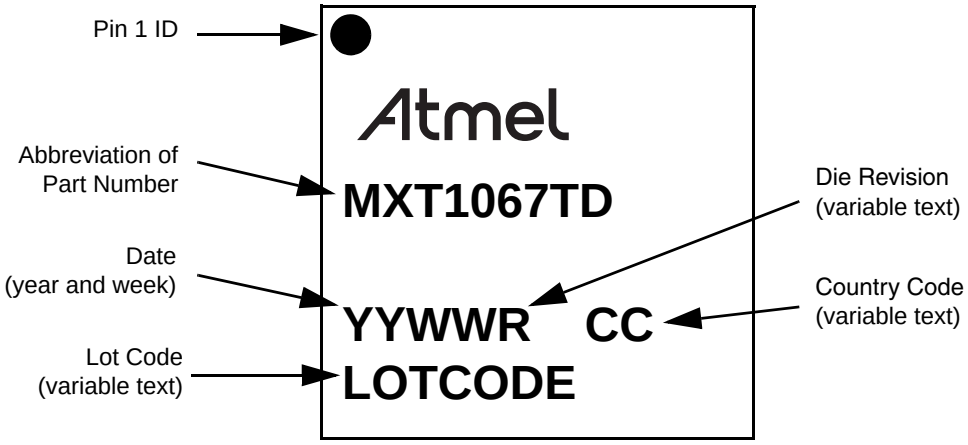
11.13 Moisture Sensitivity Level (MSL)

MSL Rating	Package Type(s)	Peak Body Temperature	Specifications
MSL3	QFP	260°C	AEC–Q100

12.0 PACKAGING INFORMATION

12.1 Package Marking Information

12.1.1 128-LEAD TQFP



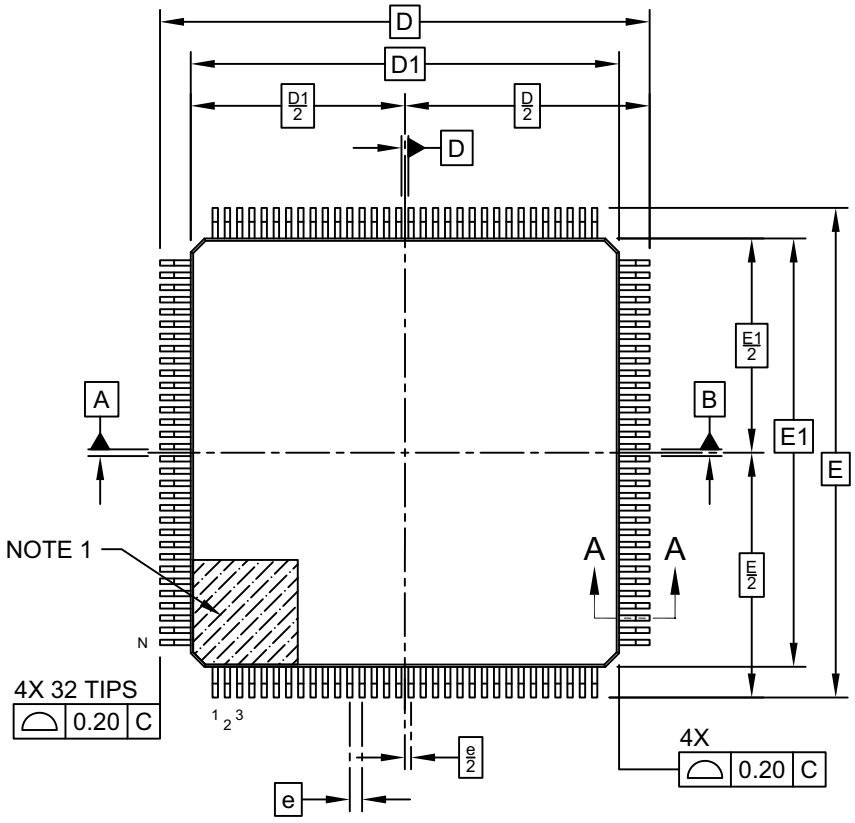
12.1.2 ORDERABLE PART NUMBERS

The product identification system for maXTouch devices is described in "Product Identification System". That section also lists example part numbers for the device.

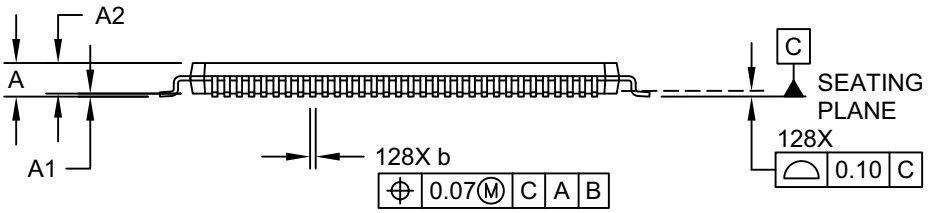
12.2 Package Details

128-Lead Thin Plastic Quad Flatpack (ZA) - 14x14 mm Body [TQFP]
SMSC Legacy VTQE3; Atmel Legacy Global Package Code APL

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW

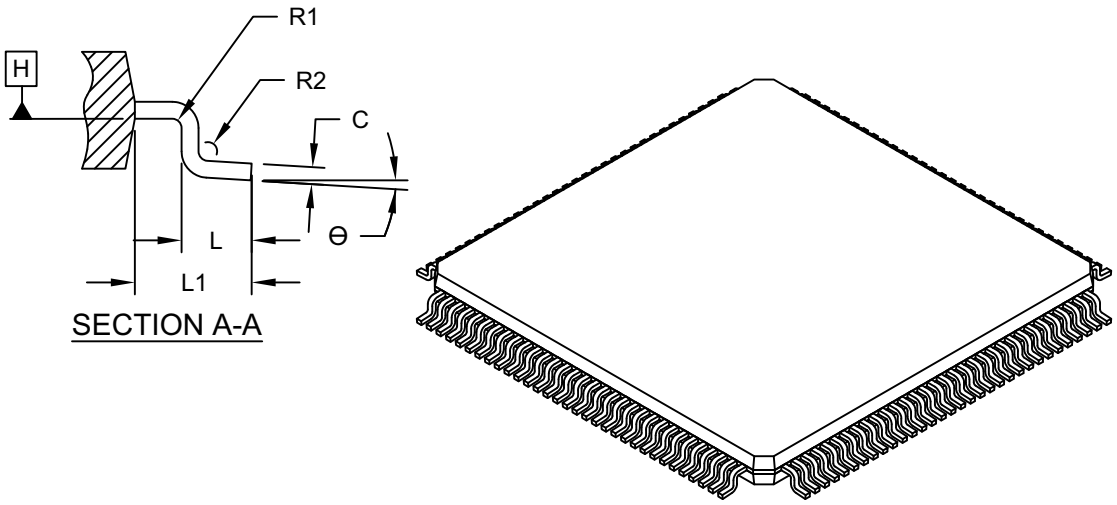


SIDE VIEW

Microchip Technology Drawing C04-181 Rev C Sheet 1 of 2

128-Lead Thin Plastic Quad Flatpack (ZA) - 14x14 mm Body [TQFP]
SMSC Legacy VTQE3; Atmel Legacy Global Package Code APL

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Leads	N		128	
Lead Pitch	e		0.40 BSC	
Overall Height	A	-	-	1.20
Standoff	A1	0.05	0.10	0.15
Molded Package Thickness	A2	0.95	1.00	1.05
Foot Length	L	0.45	0.60	0.75
Footprint	L1		1.00 REF	
Foot Angle	θ	0°	-	7°
Overall Width	E		16.00 BSC	
Overall Length	D		16.00 BSC	
Molded Package Width	E1		14.00 BSC	
Molded Package Length	D1		14.00 BSC	
Lead Width	b	0.13	0.16	0.23
Mold Draft Angle Top	C	0.09	-	0.20
Lead Bend Radius	R1	0.08	-	-
Lead Bend Radius	R2	0.08	-	0.20

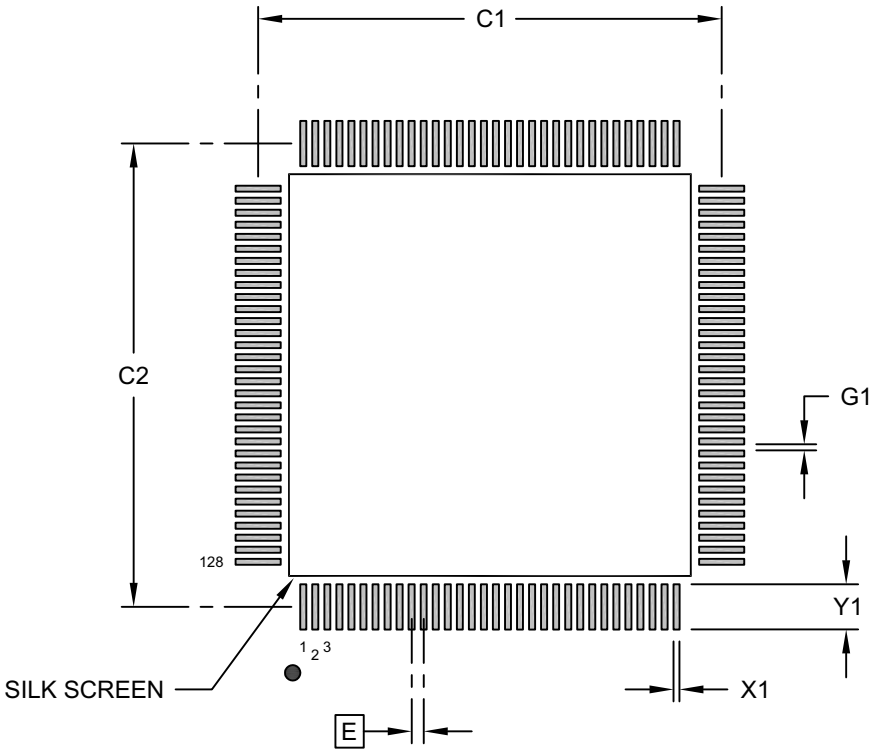
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-181 Rev C Sheet 2 of 2

128-Lead Thin Plastic Quad Flatpack (ZA) - 14x14 mm Body [TQFP]
SMSC Legacy VTQE3; Atmel Legacy Global Package Code APL

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.40 BSC	
Contact Pad Spacing	C1		15.40	
Contact Pad Spacing	C2		15.40	
Contact Pad Width (X20)	X1			0.20
Contact Pad Length (X20)	Y1			1.50
Contact Pad to Contact Pad (X124)	G1	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-2181 Rev C

APPENDIX A: ASSOCIATED DOCUMENTS

NOTE	Some of the documents listed below are available under NDA only.

The following documents are available by contacting your Microchip representative:

Product Documentation

- Application Note: MXTAN0213 – *Interfacing with maXTouch Touchscreen Controllers*

Touchscreen Design and PCB/FPCB Layout Guidelines

- Application Note: QTAN0054 – *Getting Started with maXTouch Touchscreen Designs*
- Application Note: MXTAN0208 – *Design Guide for PCB Layouts for maXTouch Touch Controllers*
- Application Note: QTAN0080 – *Touchscreens Sensor Design Guide*
- Application Note: AN2683 – *Edge Wiring for Self Capacitance maXTouch Touchscreens*

Tools

- *maXTouch Studio User Guide* (distributed as on-line help with maXTouch Studio)

APPENDIX B: REVISION HISTORY

Revision A (July 2019)

Initial edition for firmware revision 1.0.AA – Release

Revision B (August 2019)

This revision incorporates the following updates:

- Features: Automotive Application corrected to include information missing in error
- Section 7.0 “SPI Communications”: Figure 7-1 Corrected to say “Write Response”
- Section 11.7 “Touchscreen Sensor Characteristics”: Cpx specification updated with charge pump specification

INDEX

PRODUCT IDENTIFICATION SYSTEM

The table below gives details on the product identification system for maXTouch devices. See "Orderable Part Numbers" below for example part numbers for the mXT1067TD-AT/mXT1067TD-AB SPI Variant.

To order or obtain information, for example on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	–XXX	[X]	[X]	[XXX]
Device	Package	Temperature Range	Tape and Reel Option	Pattern

Device:	Base device name		
Package:	A	=	QFP (Plastic Quad Flatpack)
	AM	=	VQFN (Plastic Very Thin Quad Flat No Lead)
Temperature Range:	T	=	–40°C to +85°C (Grade 3)
	B	=	–40°C to +105°C (Grade 2)
Tape and Reel Option:	*Blank*	=	Standard Packaging (Tube or Tray)
	R	=	Tape and Reel (1)
Pattern:	Extension, QTP, SQTP, Code or Special Requirements (Blank Otherwise)		

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. See "Orderable Part Numbers" below or check with your Microchip Sales Office for package availability with the Tape and Reel option.

Orderable Part Numbers

Orderable Part Number	Firmware Revision	Description
ATMXT1067TD-ATSPIVAO (Supplied in trays)	1.0.AA	128-lead TQFP 14 × 14 × 1 mm, RoHS compliant Operating temperature range –40°C to +85°C (Grade 3)
ATMXT1067TD-ATRSPIVAO (Supplied in tape and reel)		
ATMXT1067TD-ABSPIVAO (Supplied in trays)	1.0.AA	128-lead TQFP 14 × 14 × 1 mm, RoHS compliant Operating temperature range –40°C to +105°C (Grade 2)
ATMXT1067TD-ABRSPIVAO (Supplied in tape and reel)		

THE MICROCHIP WEB SITE

Microchip provides online support via our WWW site at www.microchip.com. This web site is used as a means to make files and information easily available to customers. Accessible by using your favorite Internet browser, the web site contains the following information:

- **Product Support** – Data sheets and errata, application notes and sample programs, design resources, user's guides and hardware support documents, latest software releases and archived software
- **General Technical Support** – Frequently Asked Questions (FAQ), technical support requests, online discussion groups, Microchip consultant program member listing
- **Business of Microchip** – Product selector and ordering guides, latest Microchip press releases, listing of seminars and events, listings of Microchip sales offices, distributors and factory representatives

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CUSTOMER SUPPORT

Users of Microchip products can receive assistance through several channels:

- Distributor or Representative
- Local Sales Office
- Field Application Engineer (FAE)
- Technical Support

Customers should contact their distributor, representative or Field Application Engineer (FAE) for support. Local sales offices are also available to help customers. A listing of sales offices and locations is included in the back of this document.

Technical support is available through the web site at: http://microchip.com/support

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

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